Avenir: Managing Data Plane Diversity via Control Plane Synthesis

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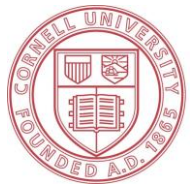
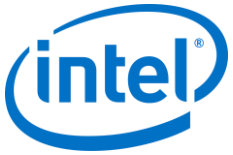
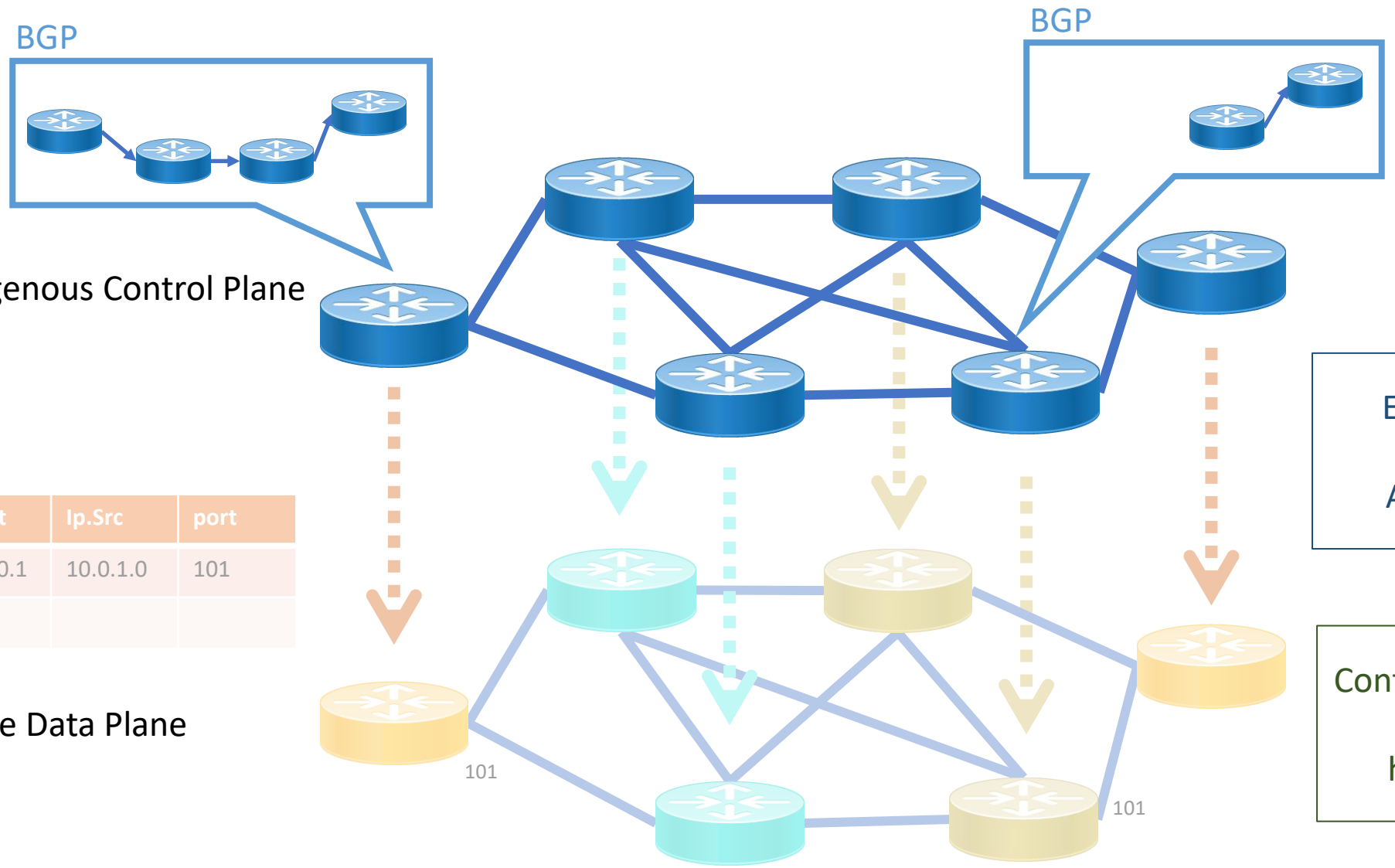






Ip.Dst	Ip.Src	port
10.0.0.1	10.0.1.0	101

Engineers work at Homogenous Abstraction Layer

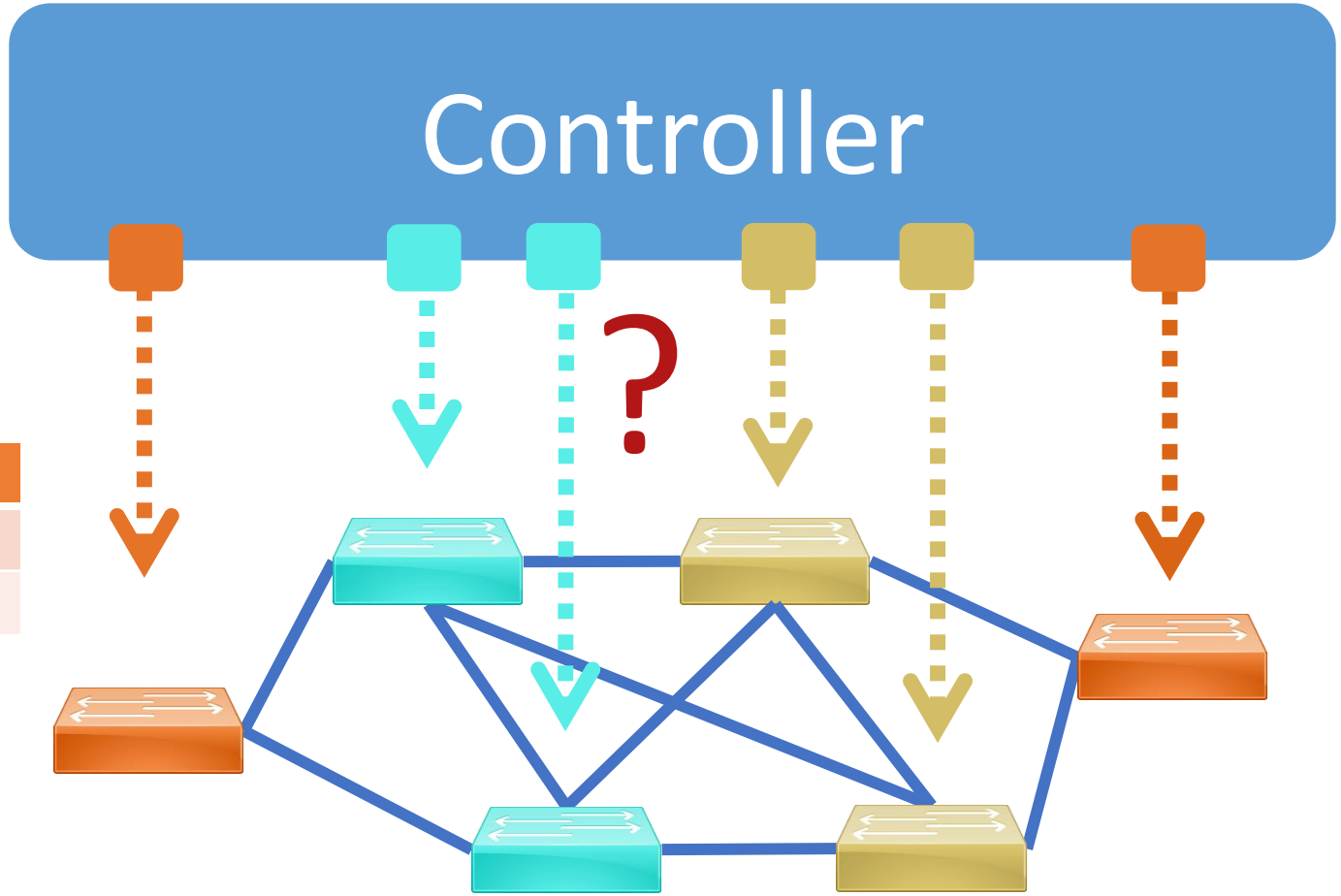
Control Plane abstraction implemented by hardware vendors

Ip.Dst	Meta
10.0.0.1	3

Ip.Src	Meta	Port
10.0.1.0	3	101

Traditional Network

Engineers manage data plane diversity



Ip.Dst	Ip.Src	port
10.0.0.1	10.0.1.0	101

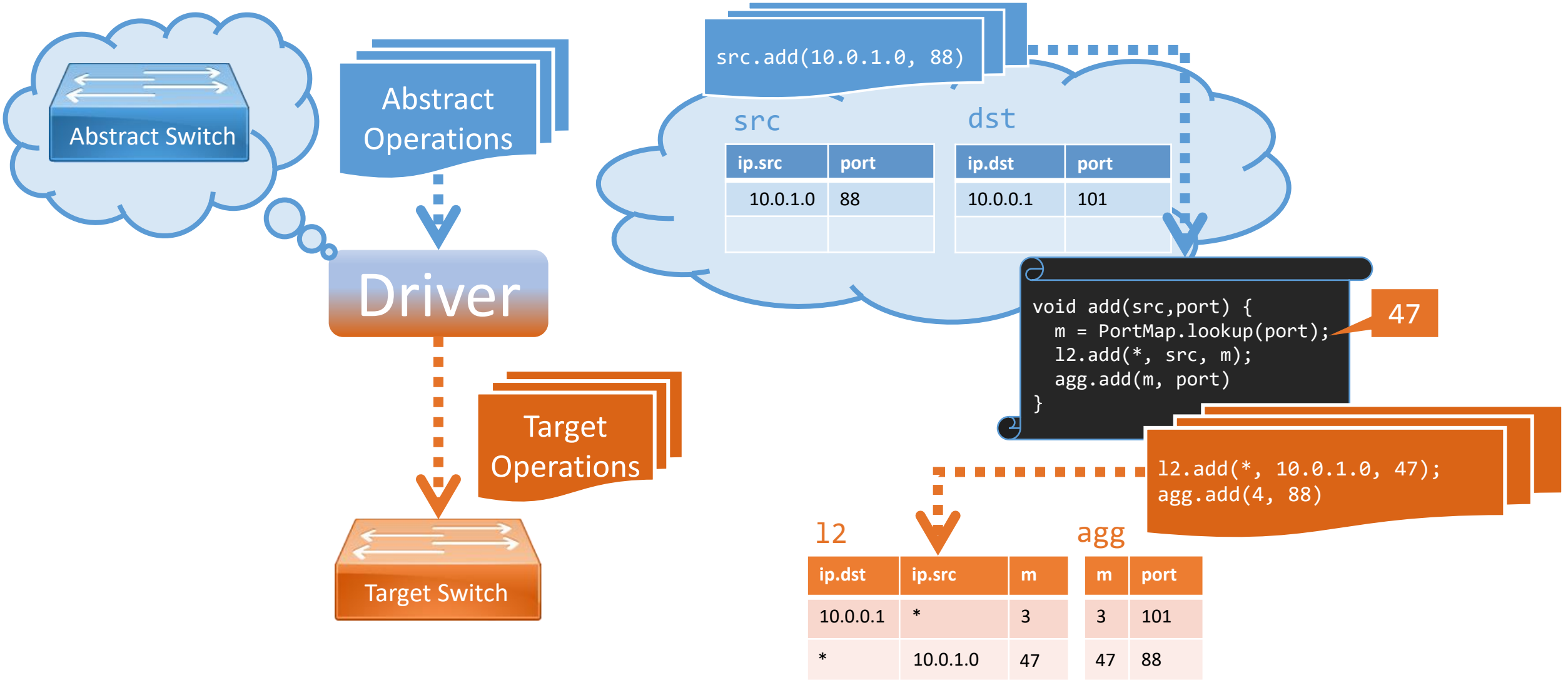
Diverse Data Plane

Software Defined Network

Ip.Dst	Meta
10.0.0.1	3

Ip.Src	Meta	Port
10.0.1.0	3	101

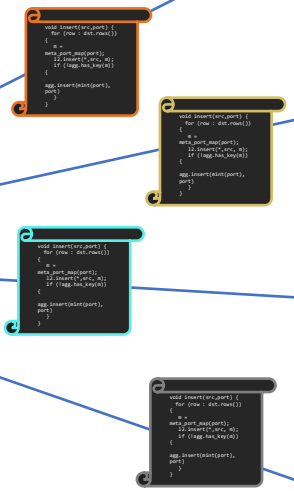
A New Driver for Every Target



Managing Drivers is Tedious

ip.src	port
10.0.1.0	CTRL

ip.dst	port
10.0.0.1	101



ip.dst	ip.src	m	m	port
10.0.0.1	*	3	3	101
*	10.0.1.0	47	47	88

ip.dst	m	ip.src	m	port
10.0.0.1	3	*	3	101
		10.0.1.0	*	88

ip.src	s	ip.dst	d	s	d	port
10.0.1.0	3	10.0.1.0	47	*	47	101
				3	*	88

ip.src	m	ip.dst	m	m	port
10.0.1.0	4	10.0.0.1	3	3	101
				4	88

Challenges

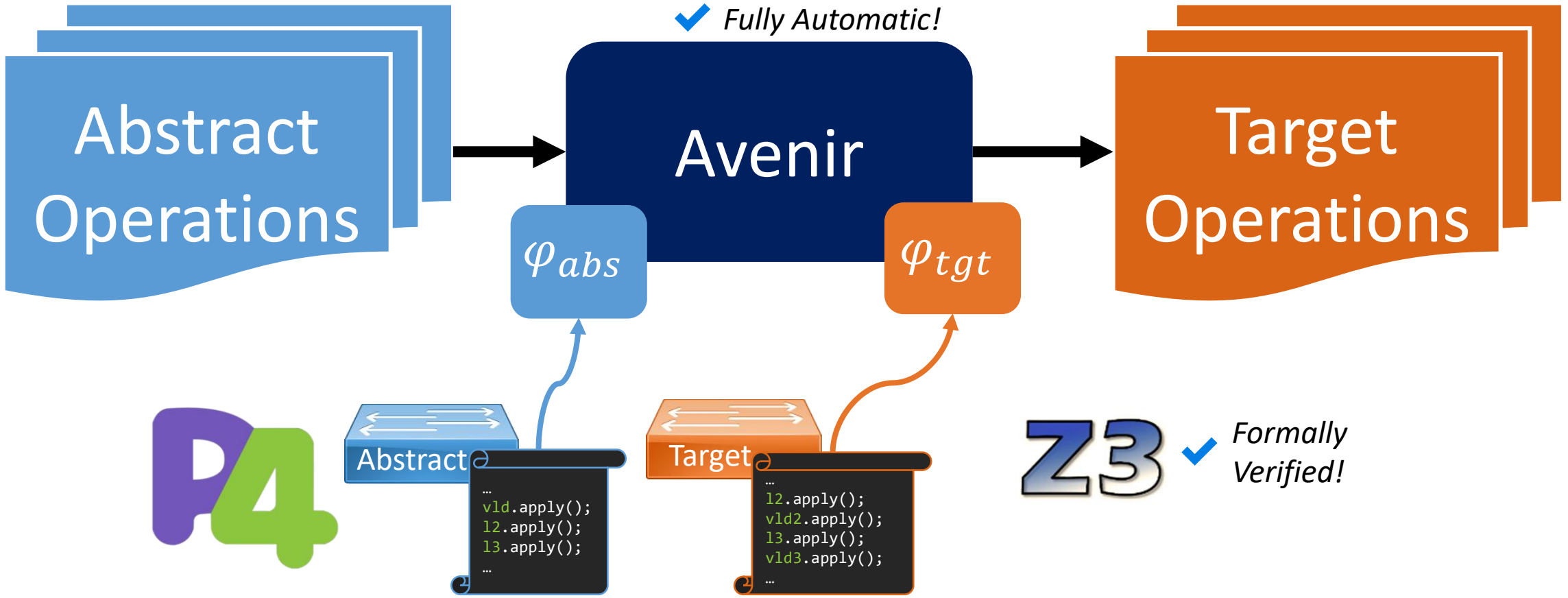
- State Management
- Scale
- Complexity
- Programmable Pipelines
- (Under)-specification

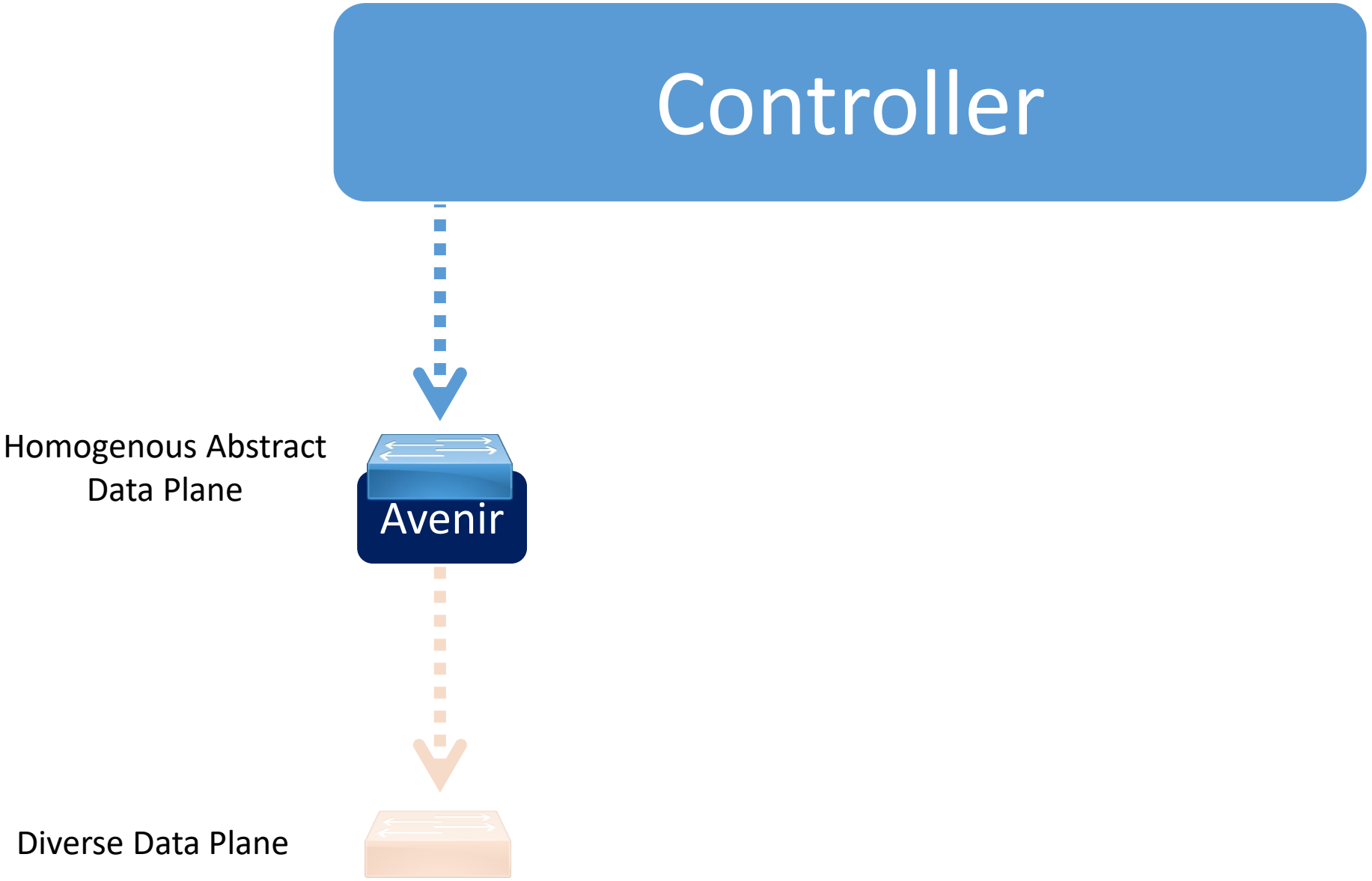
Goal:
Automatic Translation of Control Plane Operations

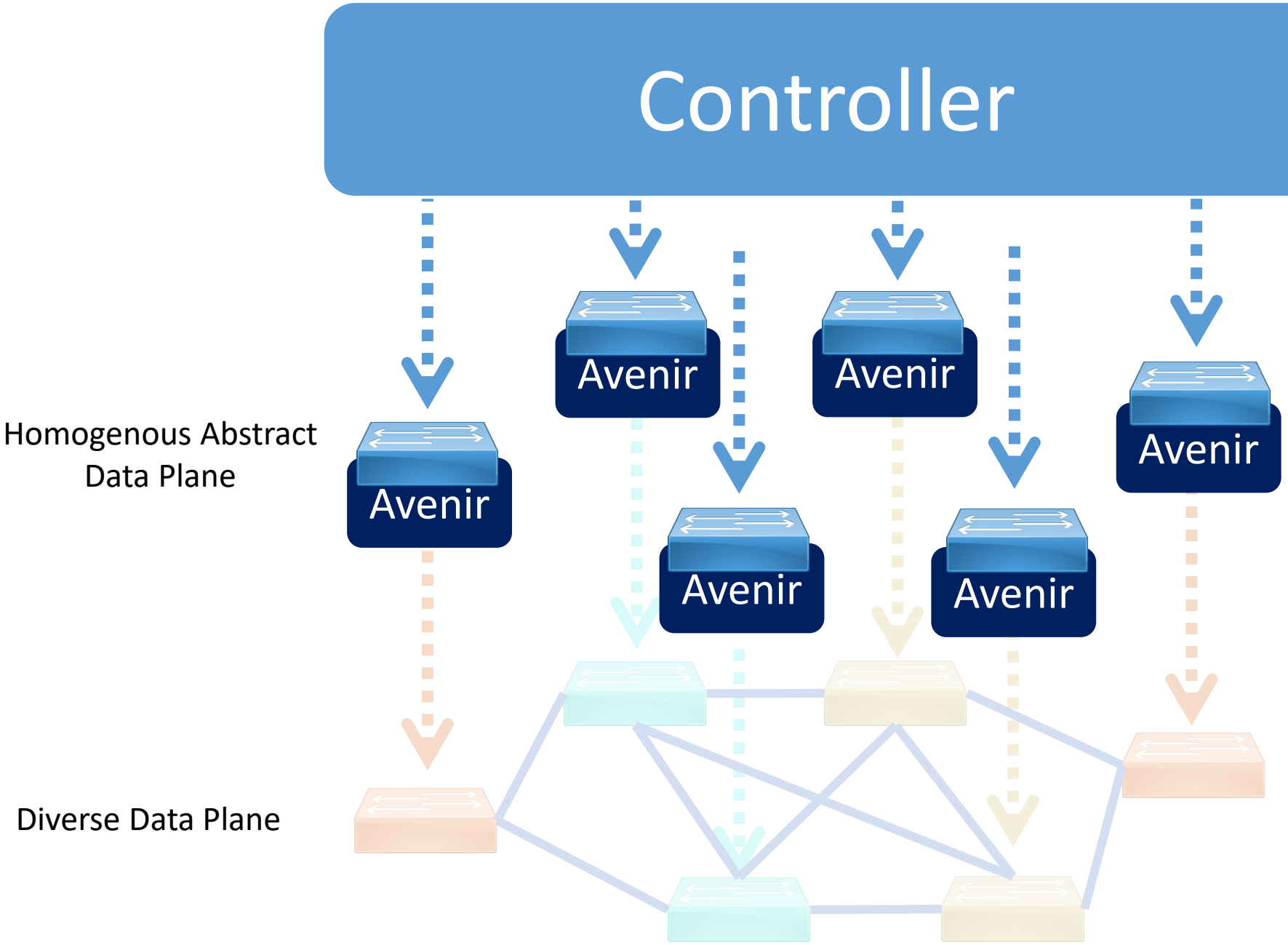
Subgoal:
Verified

Subgoal:
Efficient

Avenir: Control Plane Synthesis




Controller
Homogenous Abstract Data Plane
Avenir
Diverse Data Plane


Controller
Avenir
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Avenir
Homogenous Abstract Data Plane
Diverse Data Plane

Synthesis

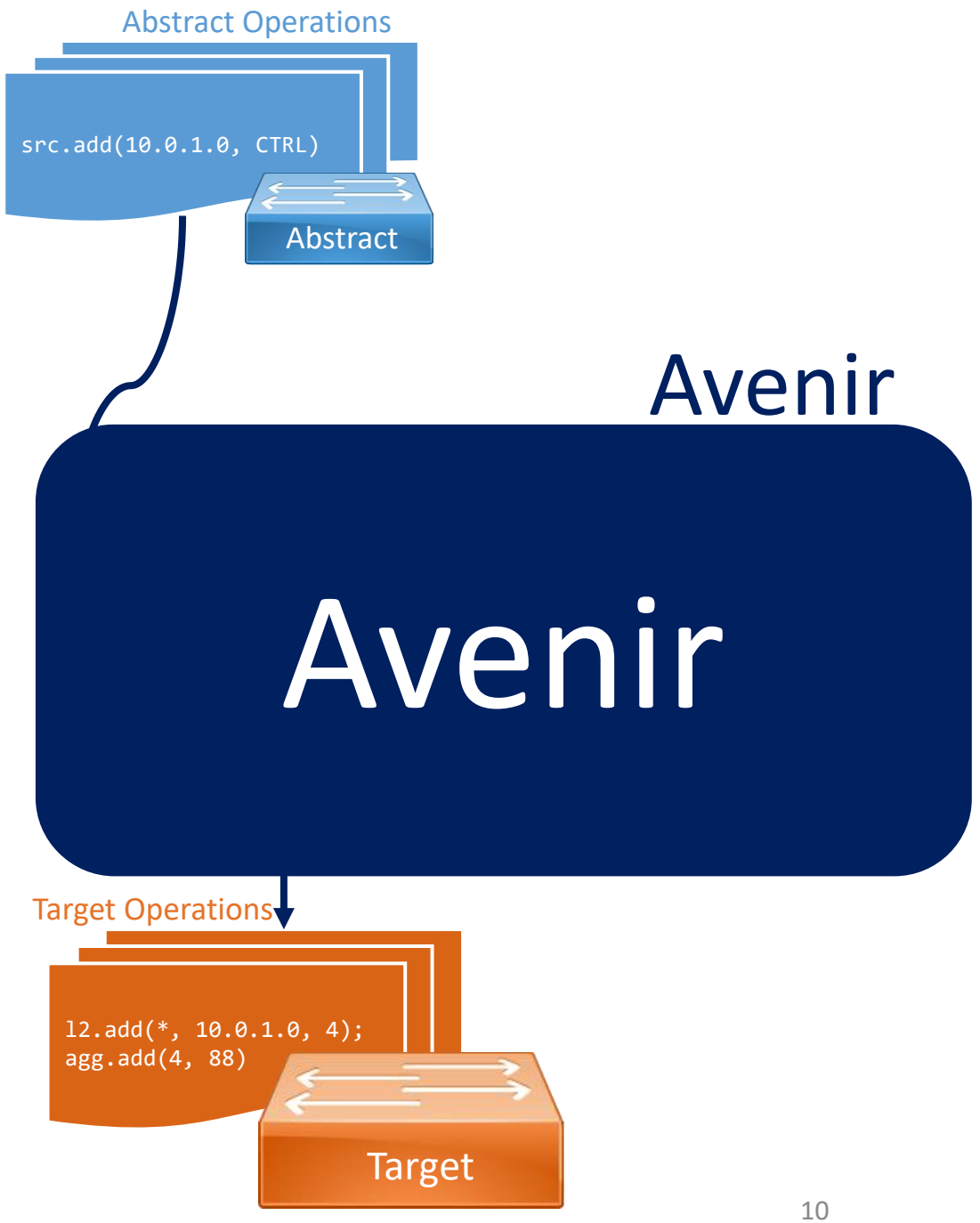
Counter-Example Guided Inductive Synthesis (CEGIS)

Theorem (**Soundness**).
Synthesized operations correctly realize abstract behavior.

Proof. Following Dijkstra '75. QED.

Theorem (**Completeness**).
If a solution exists, Avenir **eventually** computes it.

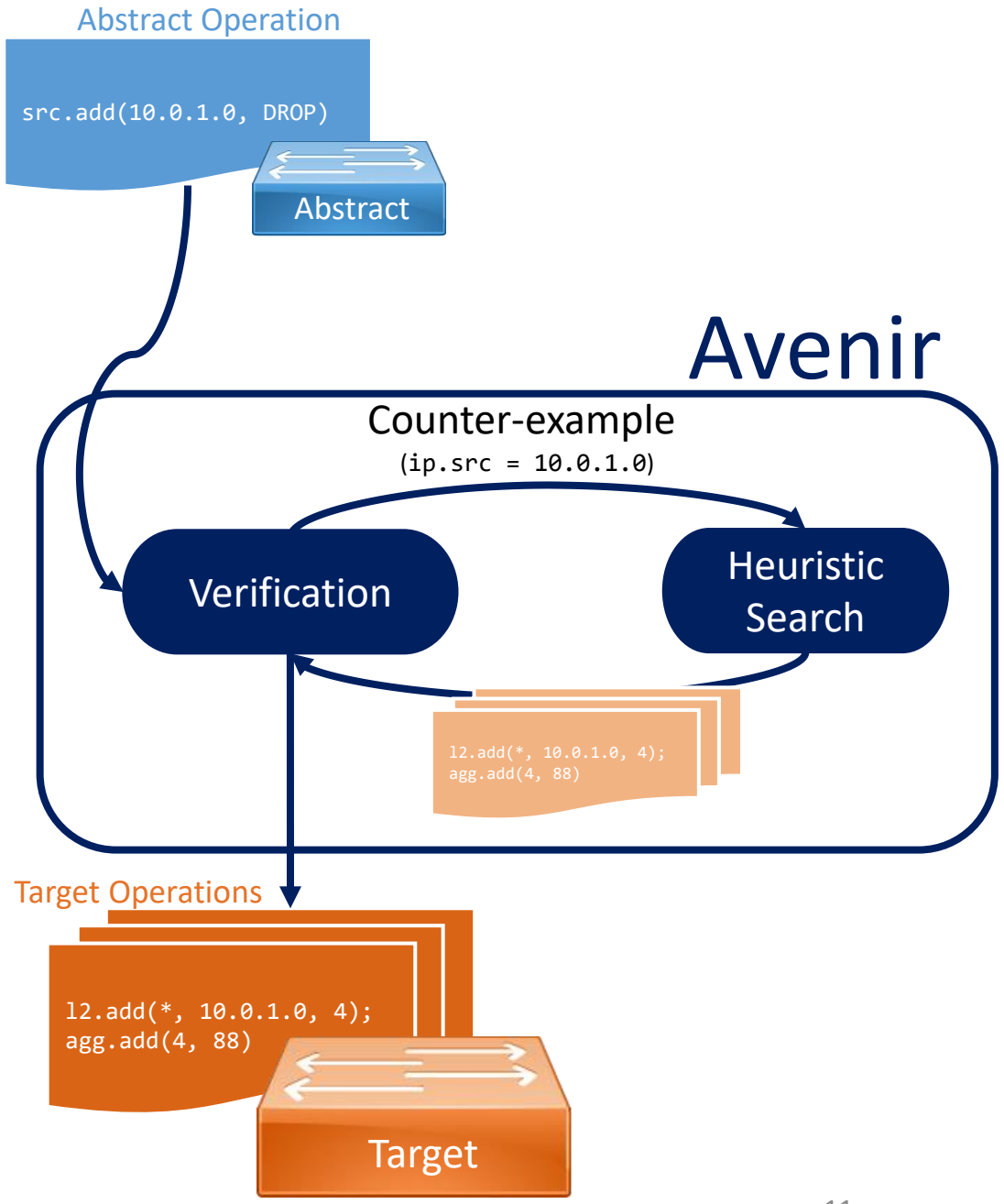
Proof.
By the finiteness of (intractably large) search space.
QED.



Making CEGIS Fast via Incremental Synthesis

- Controllers make small frequent changes
  - Process a single abstract operation at a time
  - Optimize Avenir for this common case

- Assume abstract and target behaviors are equal
  - Program Slicing
  - Static Analysis
  - Configurable Domain Specific Heuristics

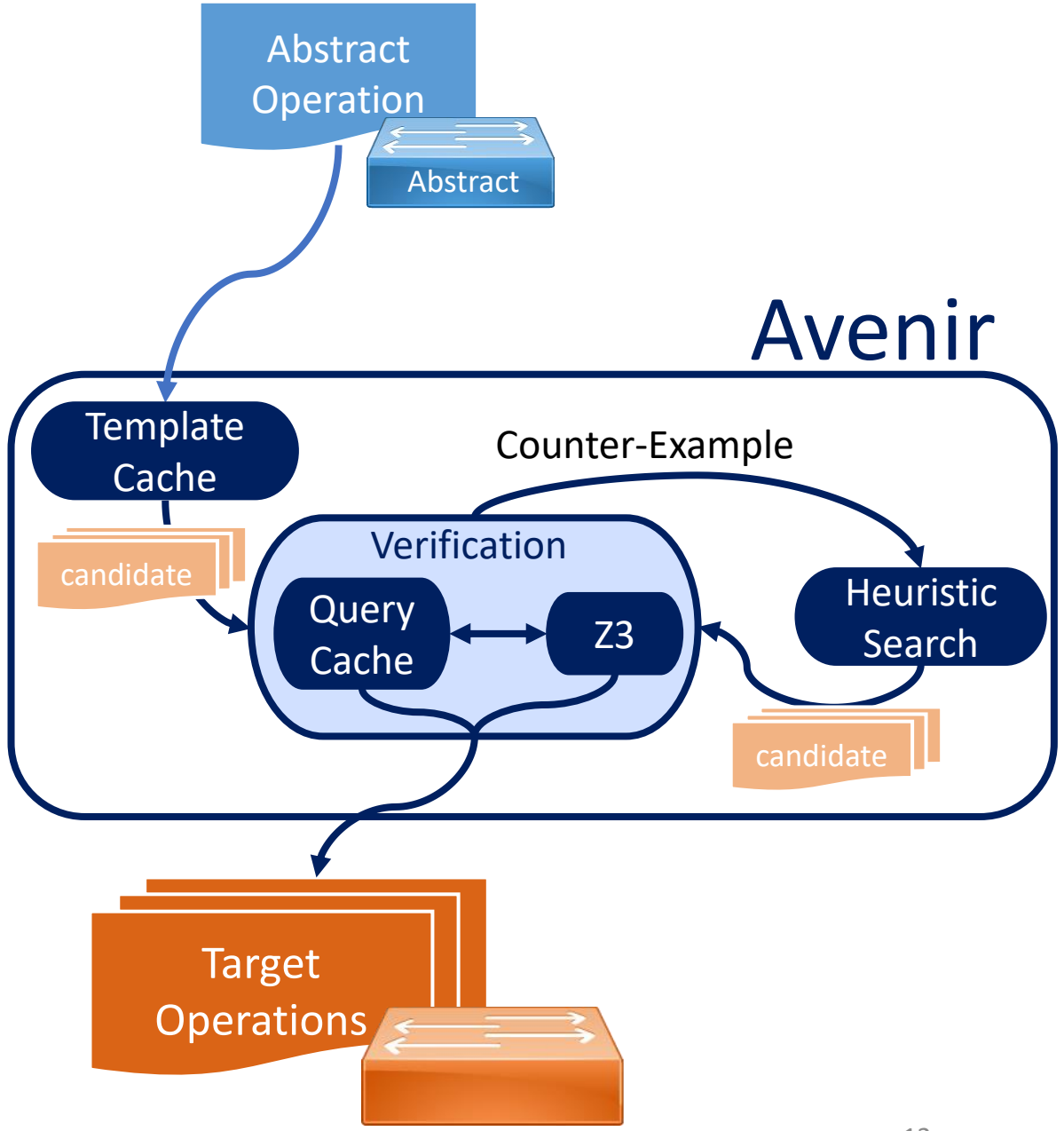


Making CEGIS Fast via Abstracting Caches

- Template Cache
  - Infers structure from previous translations
  - Replicates mapping of keys & action data
  - `src.add(ipv4.src, port)`

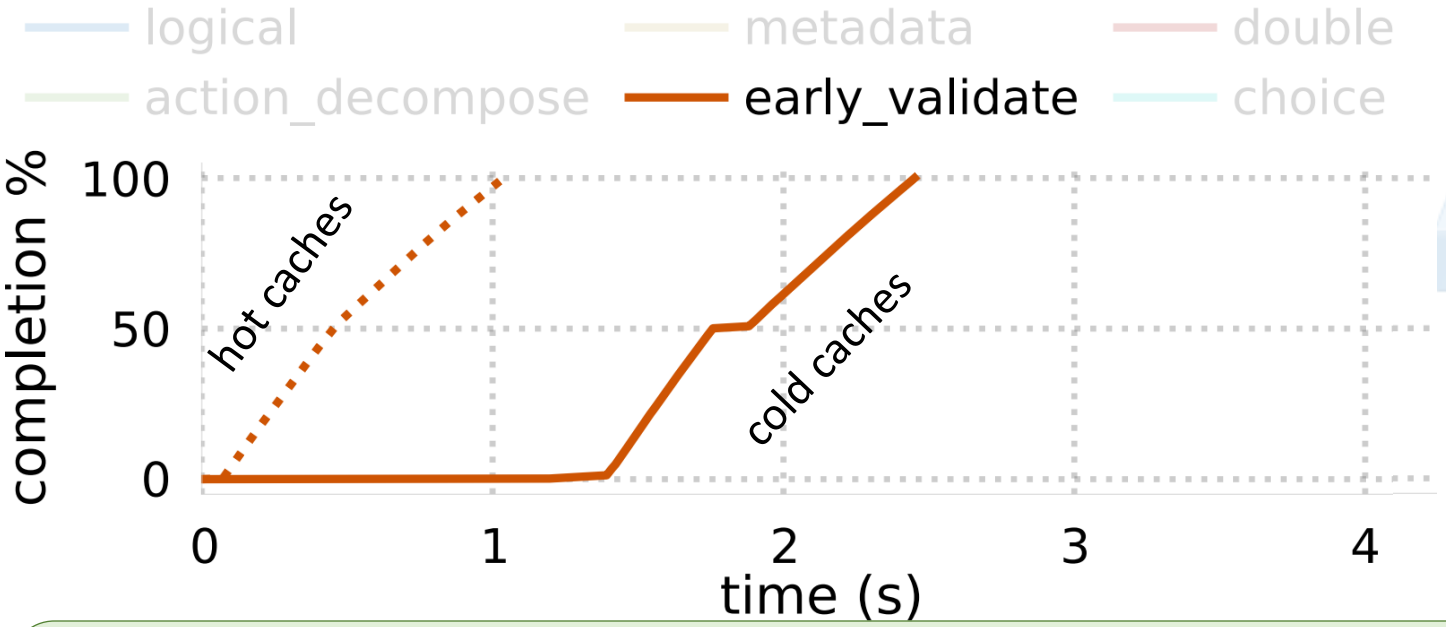
    → `l2.add(*, ipv4.src, m);`
    `agg.add(m, port)`

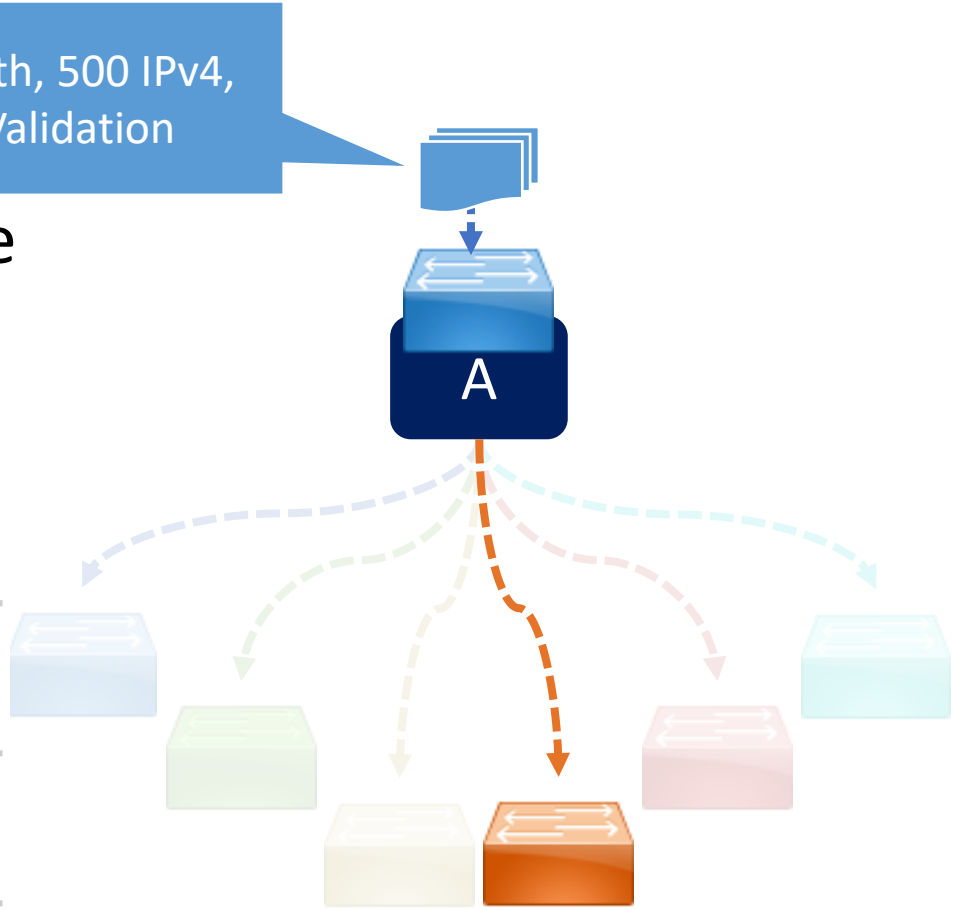
- Query Cache
  - Generalize concrete values in queries
  - $x = 5 \vee x \neq 5$ becomes $\forall b. x = b \vee x \neq b$
  - Checking $x = 47 \vee x \neq 47$ is purely syntactic



How Broad is Avenir?

- Retarget One Abstract L2/L3/Validate Pipeline
- … to various handwritten target pipelines:



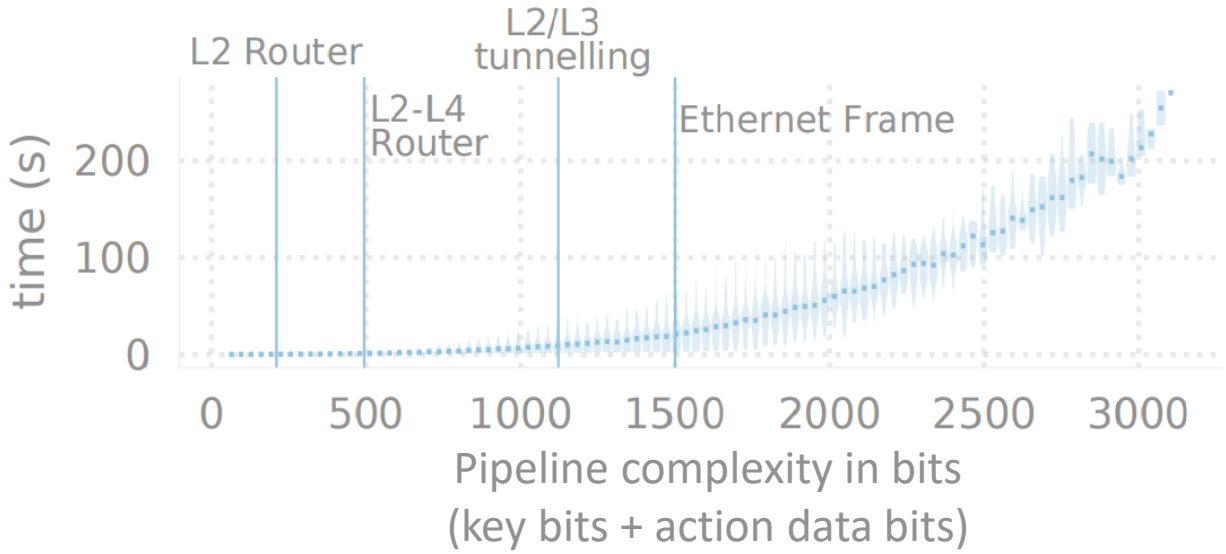


Takeaways

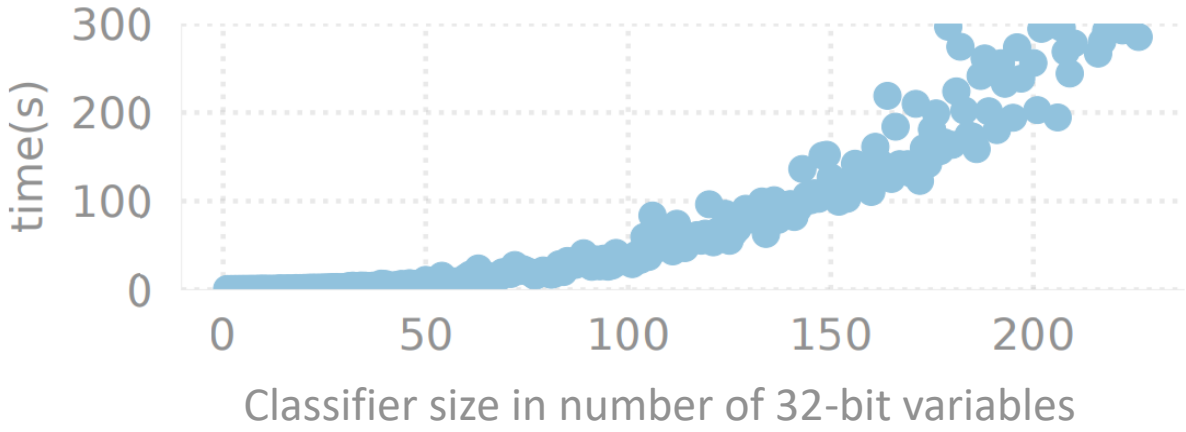
- Support diverse target pipelines
- Caches amortize the cost of learning
- Pre-populate caches for lightning-fast speeds

How Well Does Avenir Scale?

Full Program Scaling



Classifier Scaling



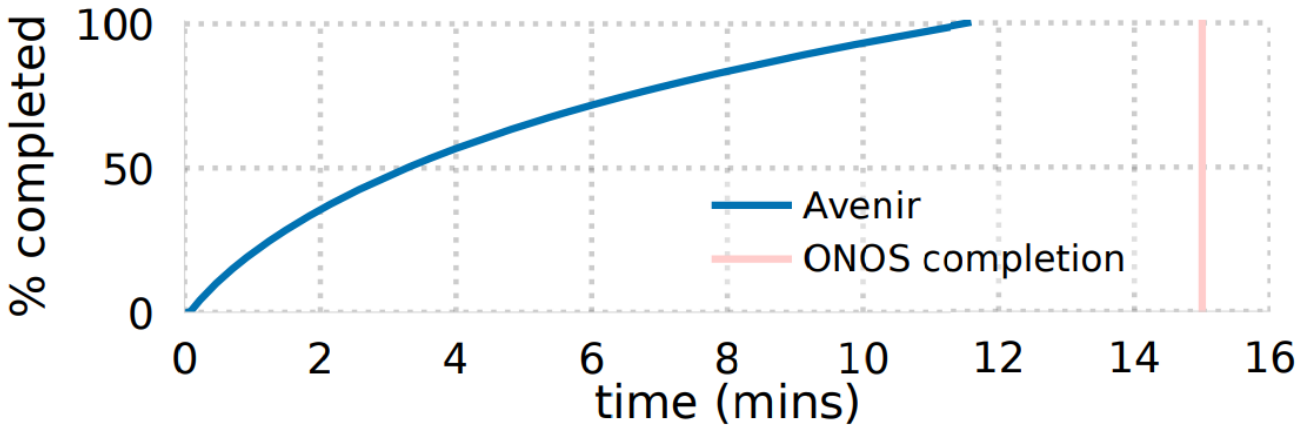
Takeaways

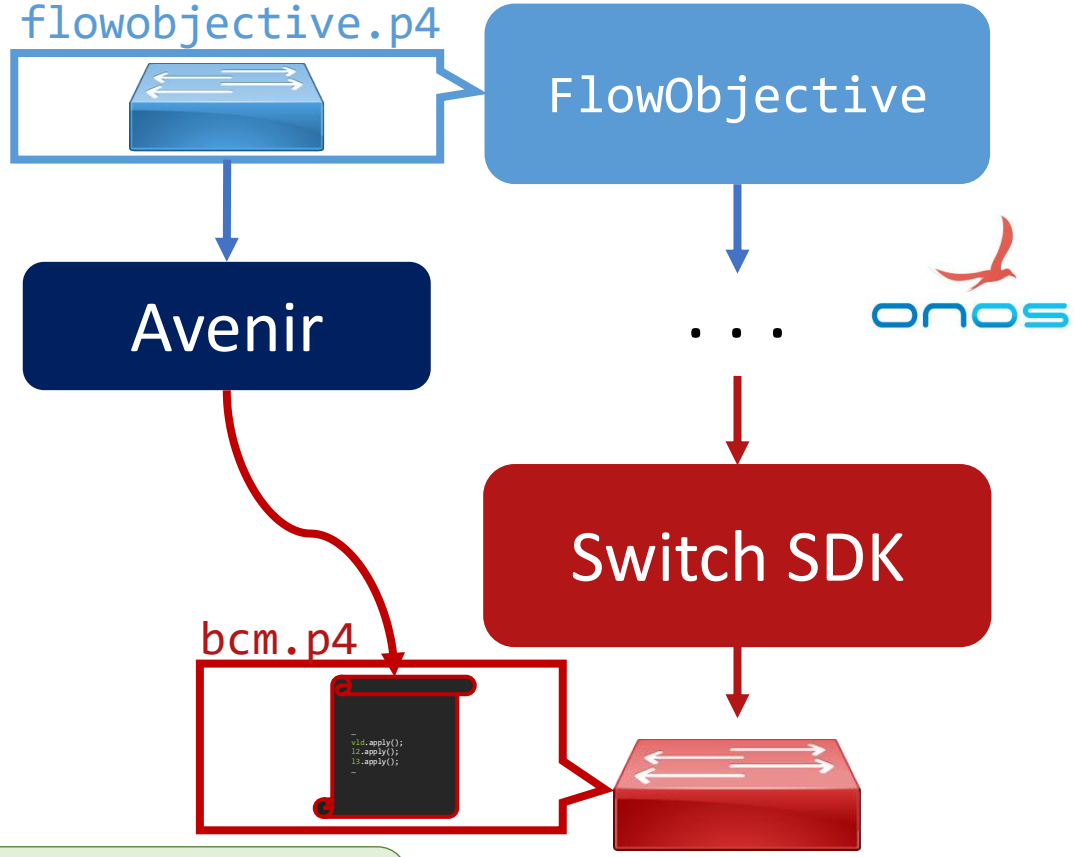
- Seems to scale exponentially
- Efficient on common program sizes
- *Results dependent on heuristics

How Efficient is Avenir In A Realistic Scenario?

- End-to-end ONOS switch reboot load test
- 40k IPv6 Routes

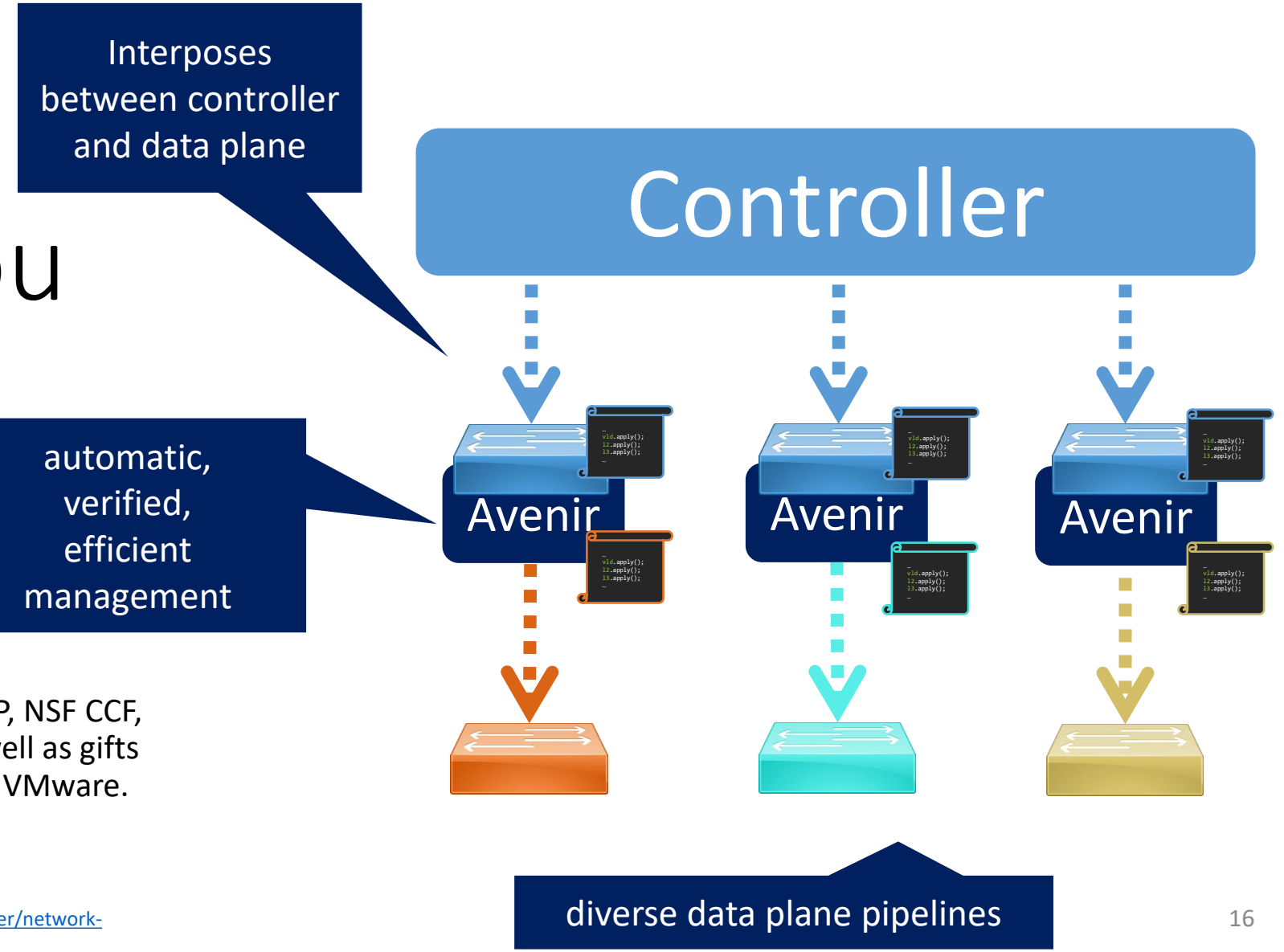
40k Routes Completion





Takeaway: Same Order of Magnitude

Thank you



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