State

CS 3410: Computer System Organization and Programming

[K. Bala, A. Bracy, G. Guidi, E. Sirer, A. Sampson, Z. Susag, and H. Weatherspoon]

Are you happy about the Superbowl

0

Yes, I am Eagles fan!

0%

No. I like KC or another team

0%

Don't care

0%

I was working on A3, Huffman Compression!

0%

Big Picture: How to Design a Processor

C

```
int x = 10;
x = 2 * x + 15;
```

compiler

How does add work?

RISC-V assembly language

```
addi x5, x0, 10      x5 = x0 + 10
muli x5, x5, 2       x5 = x5 * 2
addi x5, x5, 15      x5 = x5 + 15
```

x0 = 0

assembler

RISC-V machine language

```
000000001010 00000 000 00101 0010011
00000000001000101001001010011111
000000001111 00101 000 00101 0010011
```

10 x0 x5 op = addi

15 x5 x5 op = addi

EVERYTHING IS A NUMBER!

Big Picture: How to Design a Processor

C

```
int x = 10;
x = 2 * x + 15;
```

compiler

How does add work?

RISC-V assembly language

```
addi x5, x0, 10     <-- x5 = x0 + 10
slli x5, x5, 1      <-- x5 = x5 * 2
addi x5, x5, 15     <-- x5 = x5 + 15
```

x0 = 0

assembler

RISC-V machine language

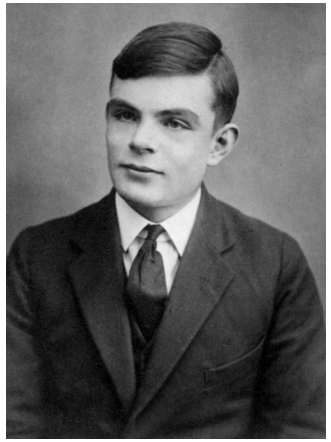
```
00000000101000000000001010010011
00000000000100101001001010011111
00000000111100101000001010010011
```

10 x0 x5 op = addi

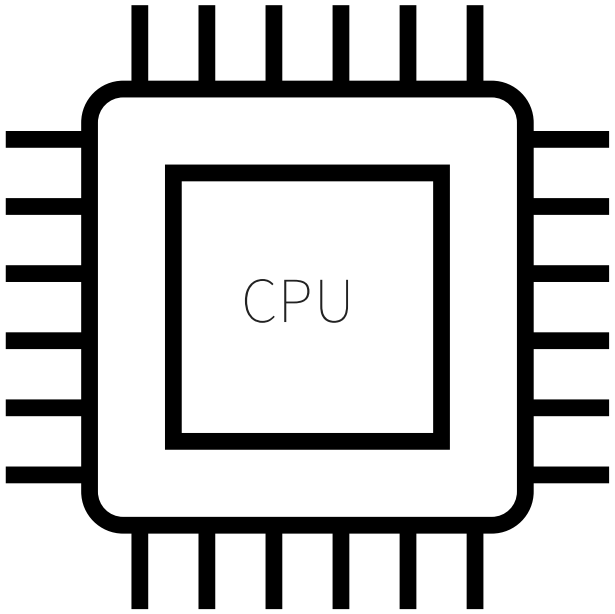
15 x5 x5 op = addi

EVERYTHING IS A NUMBER!

Big Picture: How to Design a Processor

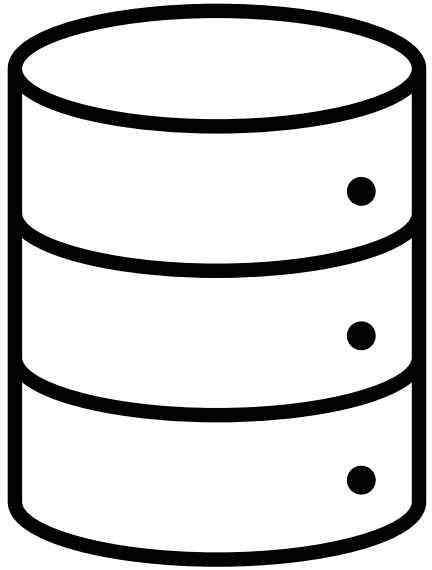


Processor



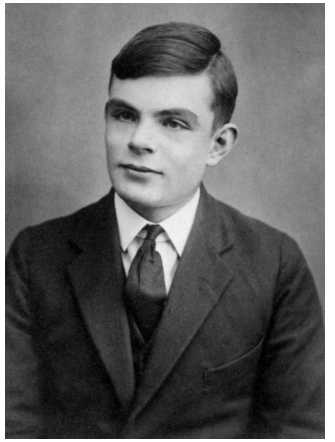
- ☑ Runs code; does computations
- ☒ Doesn't remember anything

Memory

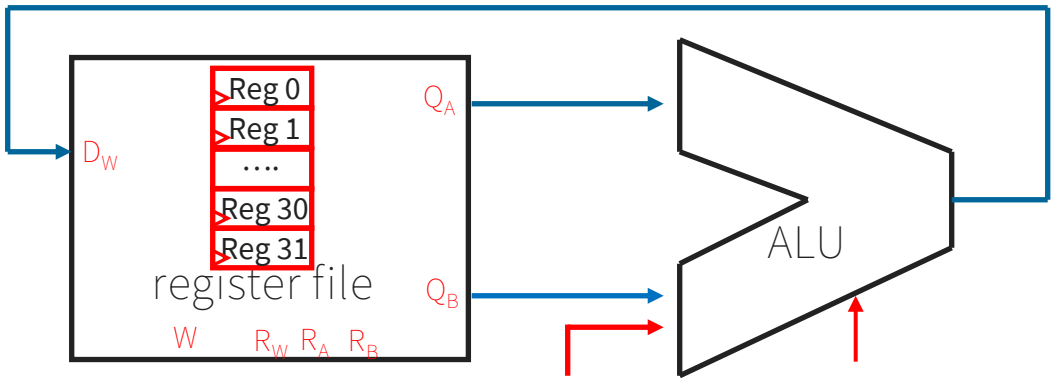


- ☒ Can't compute anything
- ☑ Stores data

Big Picture: How to Design a Processor



Processor



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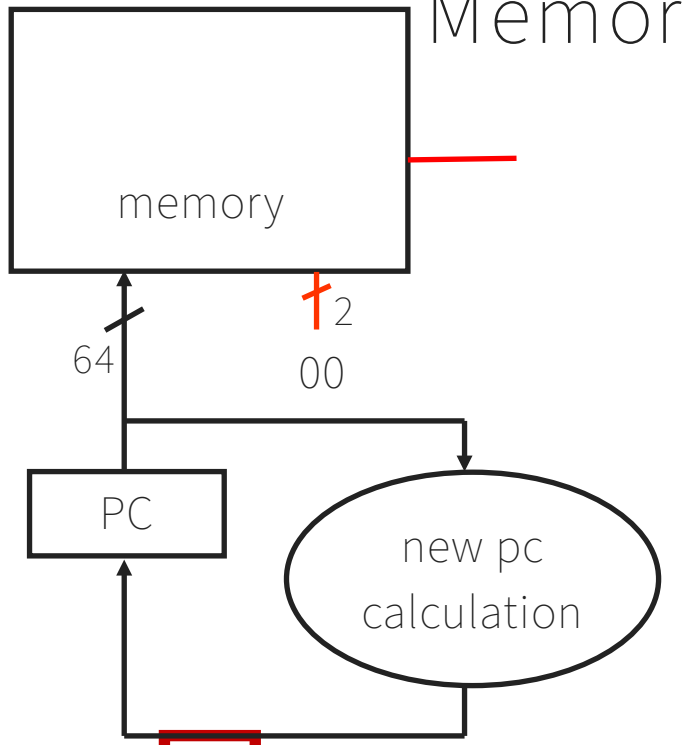

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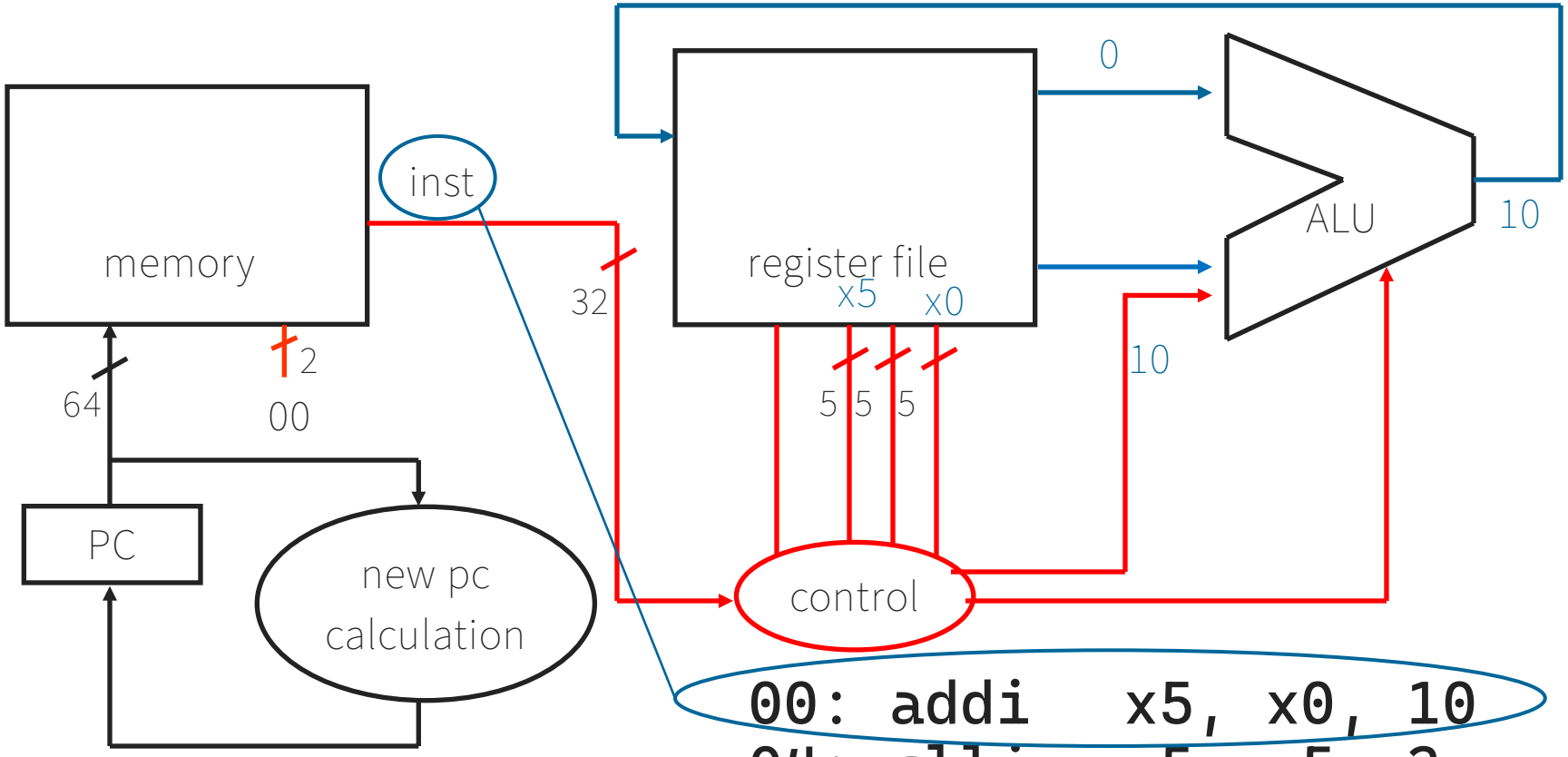
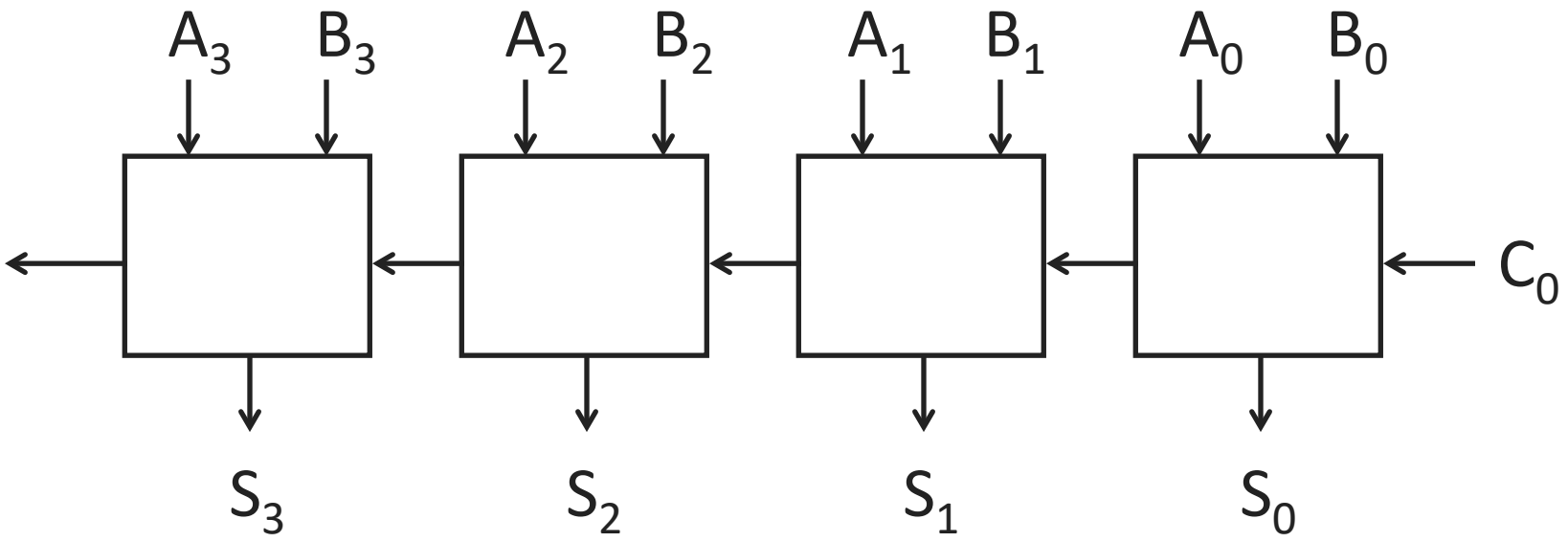
Big Picture: How to Design a Processor



Review

- We can generalize 1-bit Full Adders to 32 bits, 64 bits …



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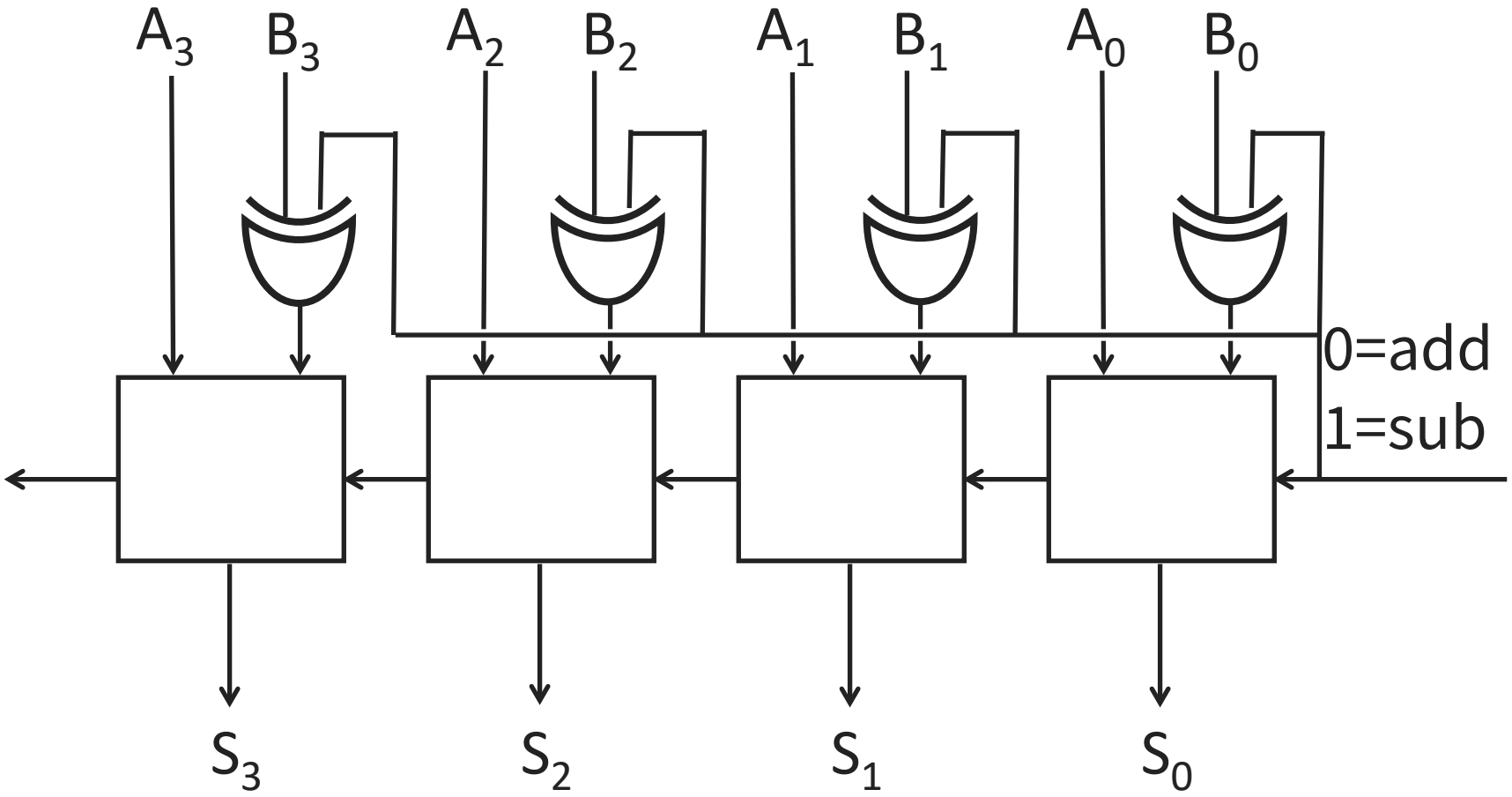

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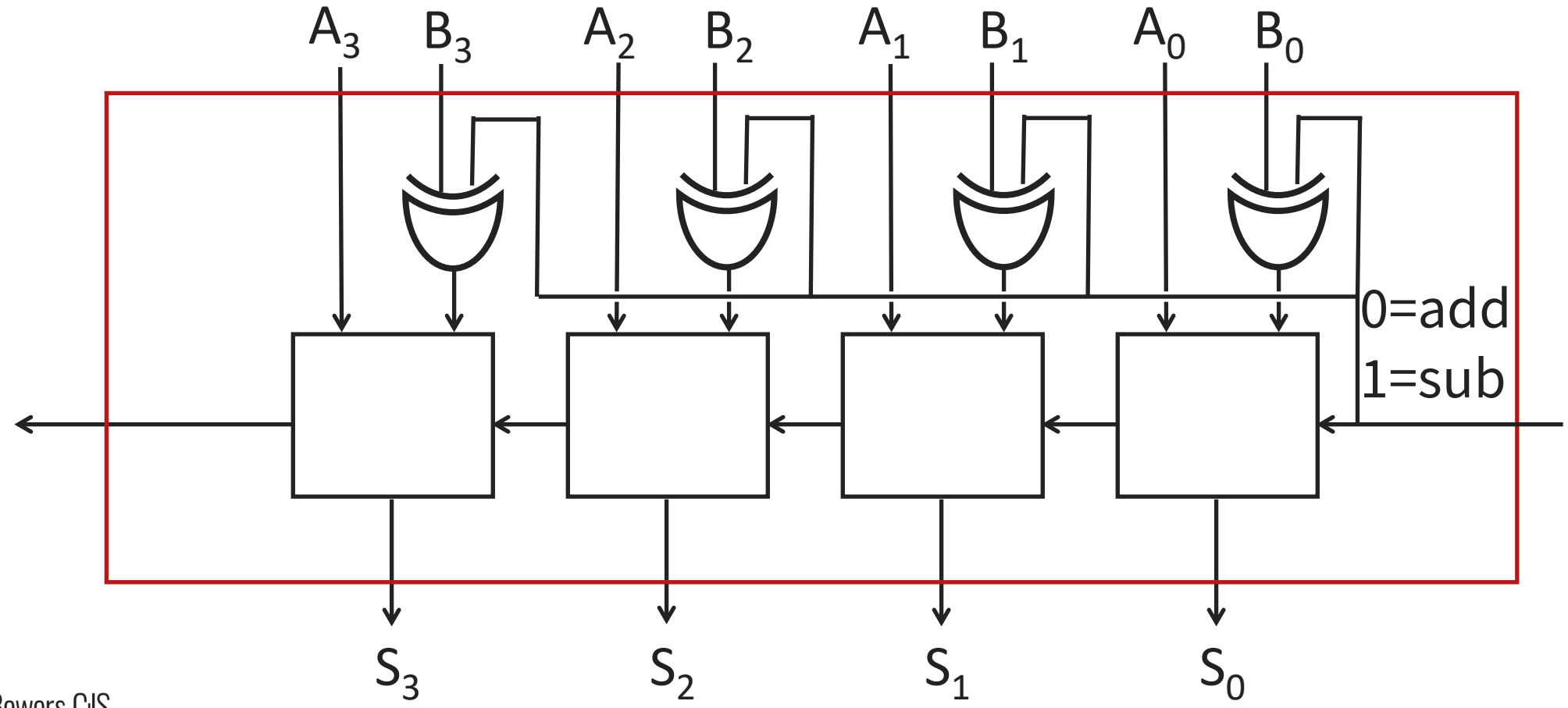

Review

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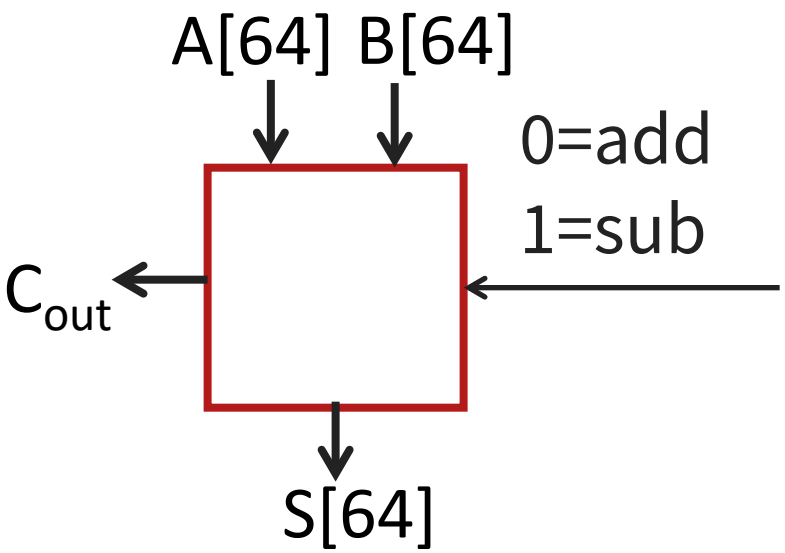
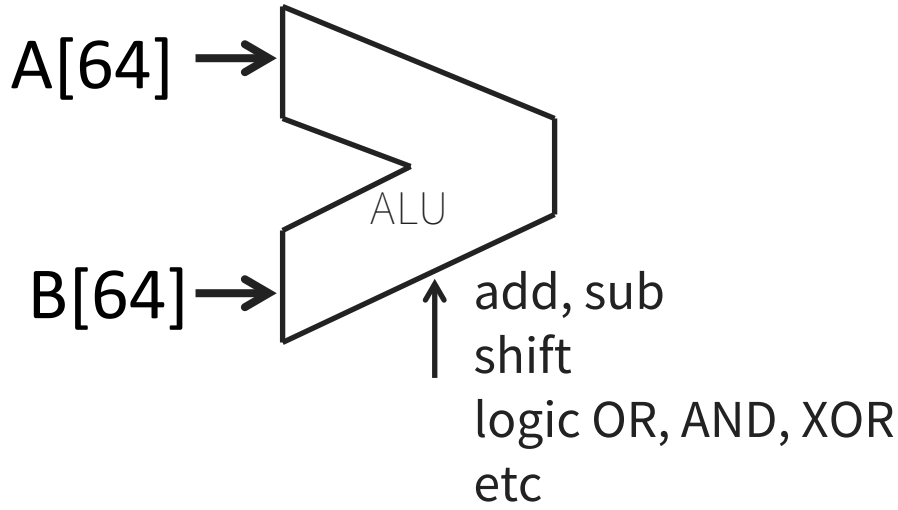


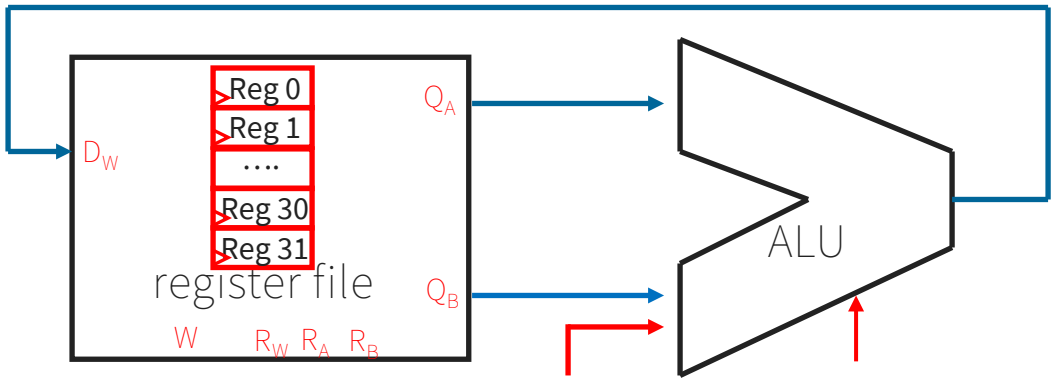
Review

- We can generalize 1-bit Full Adders to 32 bits, 64 bits …
- Arithmetic Logic Unit (ALU) adds, subtracts, shifts, logic OR, AND, XOR, etc



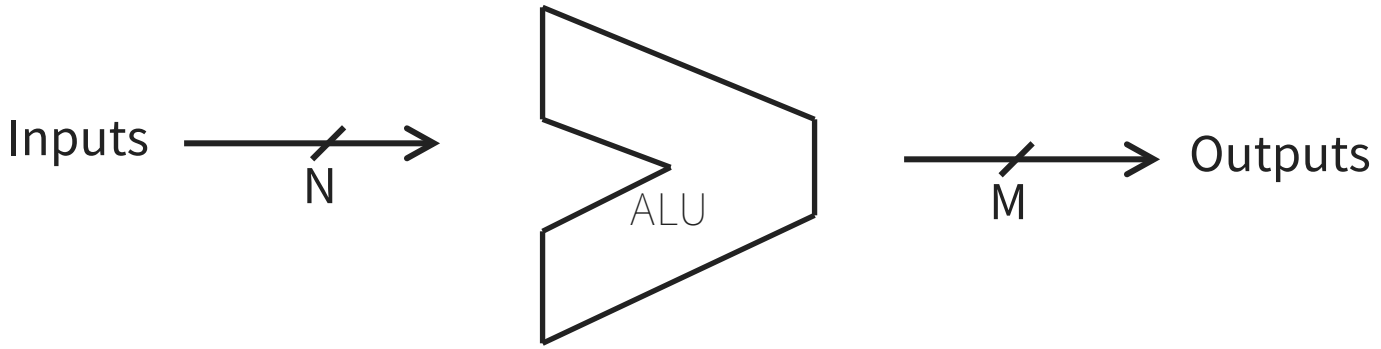
Goal for today

- How do we store results



Stateful Components

- Until now is combinational logic
  - Output is computed when inputs are present
  - System has no internal state
  - Nothing computed in the present can depend on what happened in the past!



- Need a way
  - to record data
  - to build stateful circuits
  - state-holding device

Stateful Components

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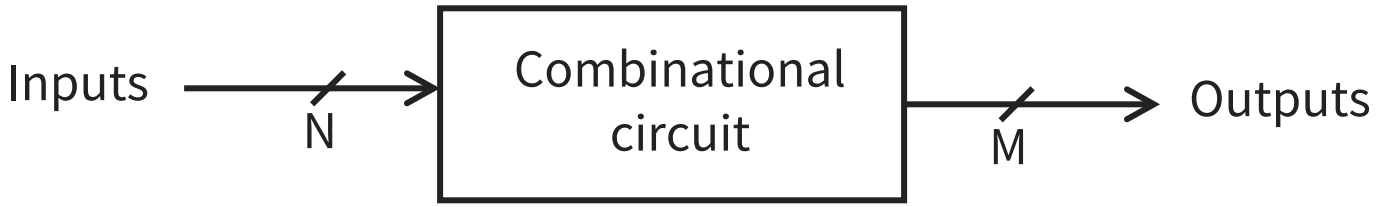


- Need a way
  - to record data
  - to build stateful circuits
  - state-holding device

Goals for Today

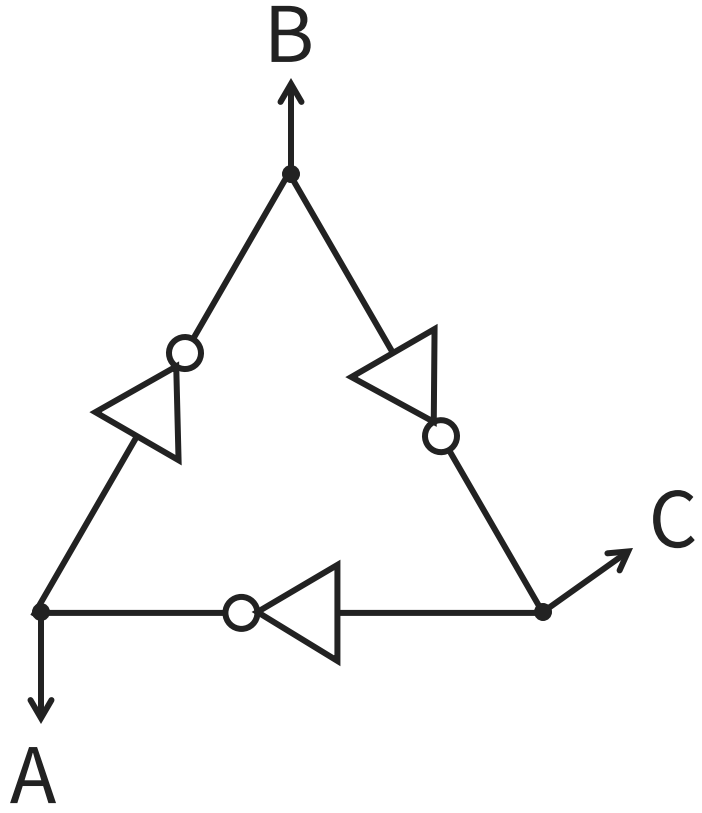
State

- How do we store one bit?
- Attempts at storing (and changing) one bit
  - Set-Reset Latch
  - D Latch
  - D Flip-Flops
- How do we store N bits?
  - Register: storing more than one bit, N-bits

Goal

How do we store store one bit?

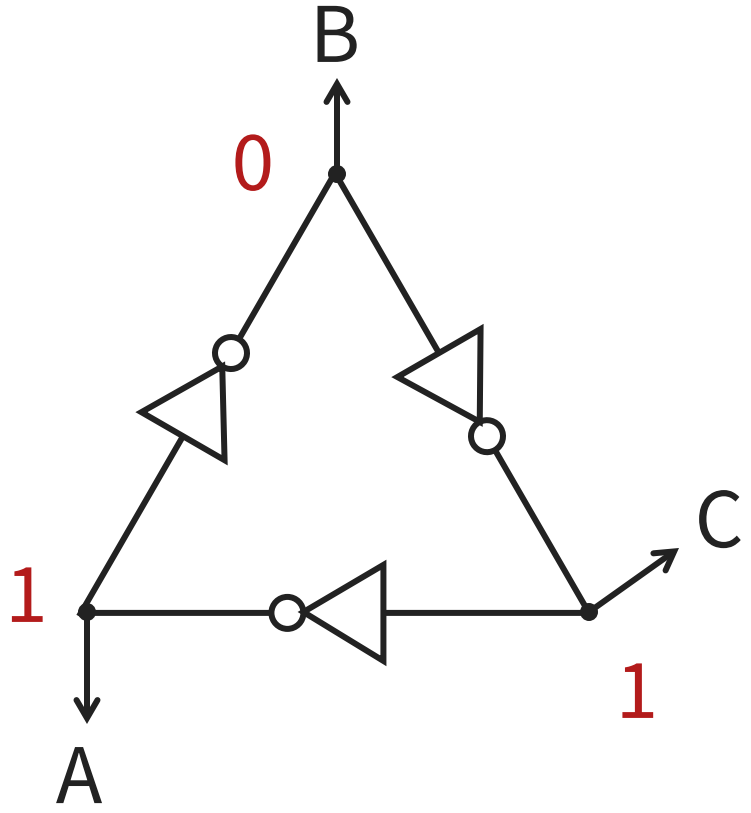
First Attempt: Unstable Devices



First Attempt: Unstable Devices

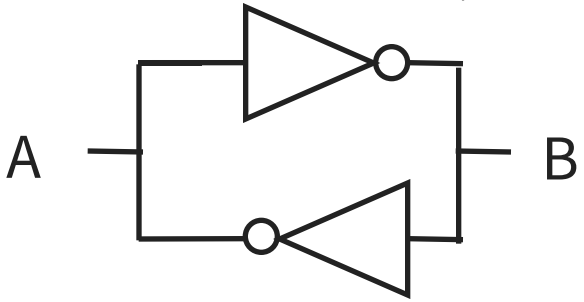
Does not work!

- Unstable
- Oscillates wildly!



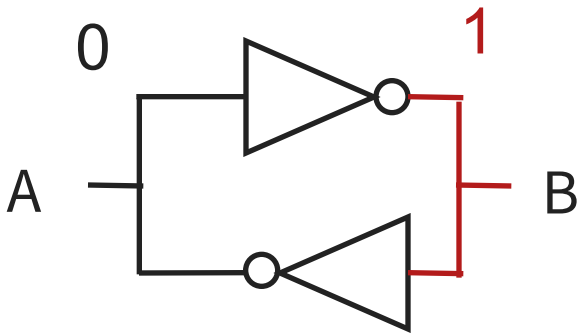
Second Attempt: Bistable Devices

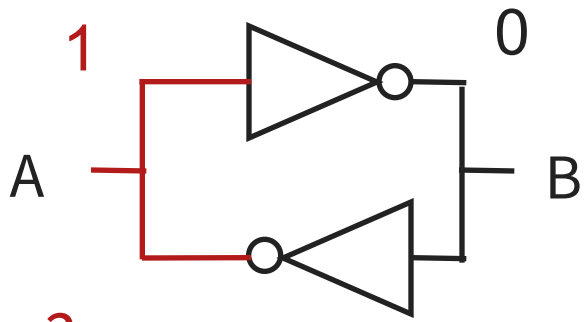
- Stable and unstable equilibria?



A Simple Device

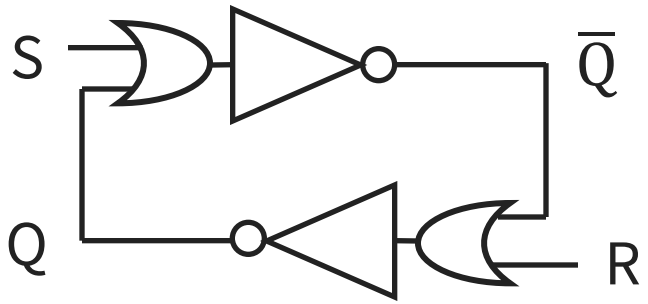
In stable state, A != B



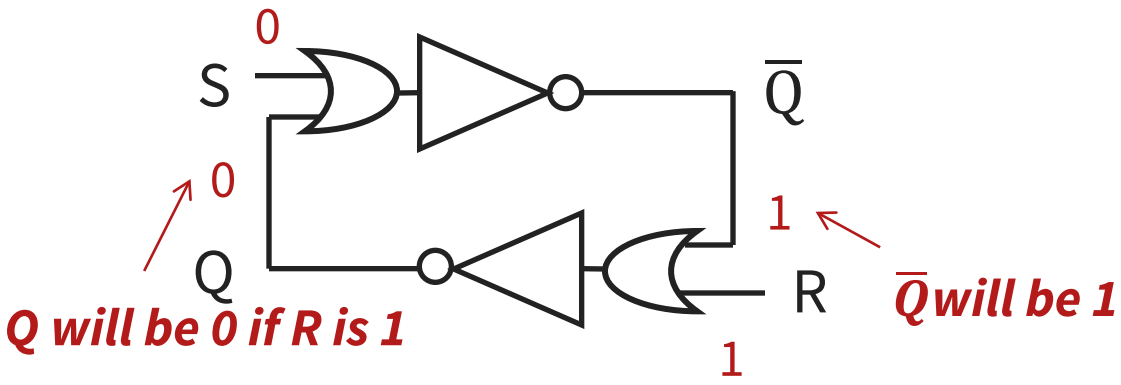


How do we change the state?

Third Attempt: Set-Reset Latch



Third Attempt: Set-Reset Latch



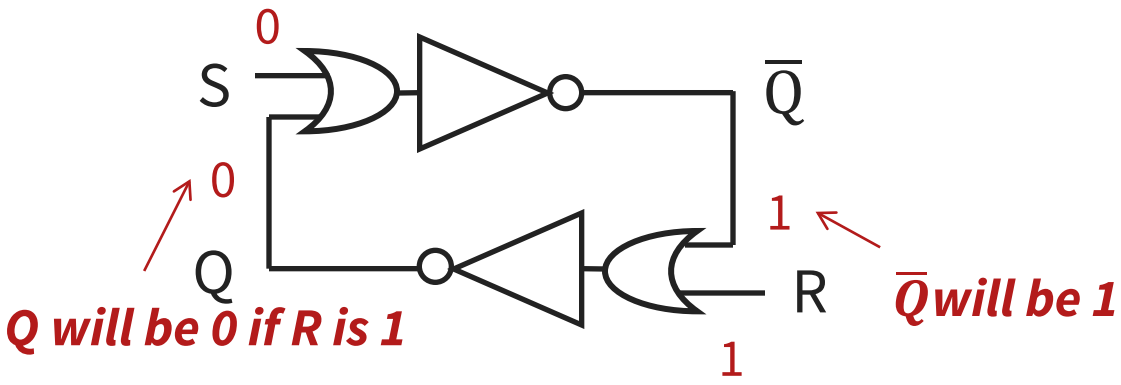
A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0		
0	1		
1	0		
1	1		

Set-Reset (S-R) Latch

Stores a value Q and its complement

Third Attempt: Set-Reset Latch



A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
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S	R	Q	$\overline{Q}$
0	0		
0	1	0	1
1	0		
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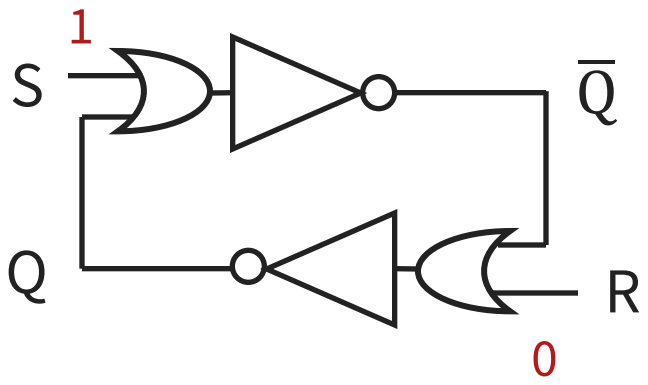


A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0		
0	1	0	1
1	0	?	?
1	1		

Set-Reset (S-R) Latch

Stores a value Q and its complement

What are the values for Q and $\overline{Q}$?

a) 0 and 0
b) 0 and 1
c) 1 and 0
d) 1 and 1

PollEV Question

What are the values for Q and !Q?

0

0 and 0

0%

0 and 1

0%

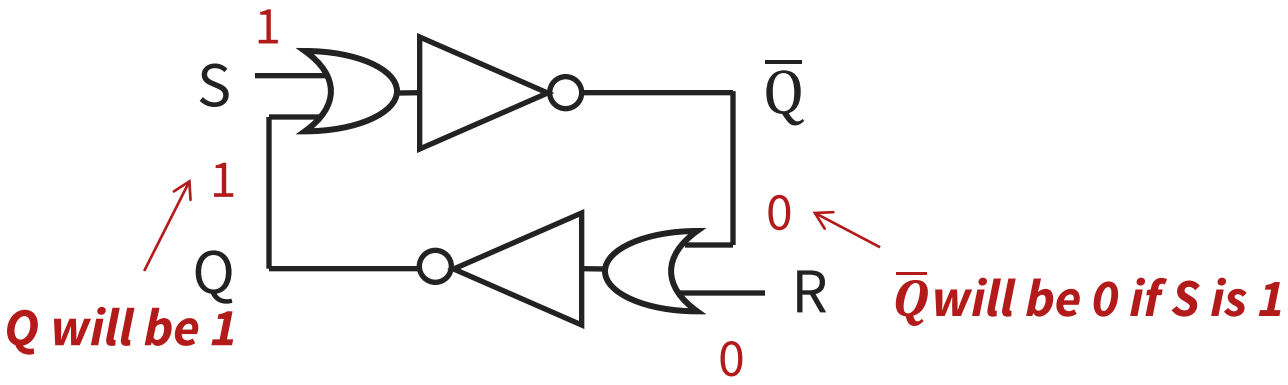
1 and 0

0%

1 and 1

0%

Third Attempt: Set-Reset Latch



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0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0		
0	1	0	1
1	0	1	0
1	1		

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PollEV Question

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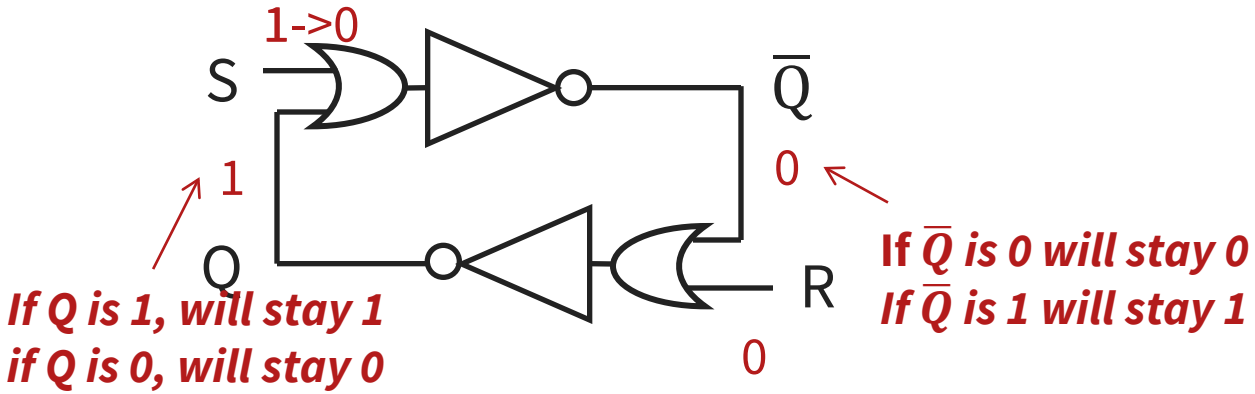
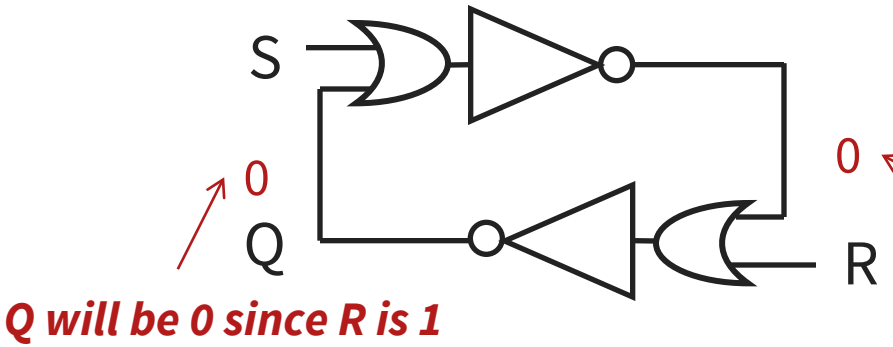


A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1		

Set-Reset (S-R) Latch
Stores a value Q and its complement

Third Attempt: Set-Reset Latch



A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	?	?

Set-Reset (S-R) Latch
Stores a value Q and its complement

What happens when S,R changes from 1,1 to 0,0?

What's wrong with the SR Latch? PollEV Question

A. Q is undefined when S=1 and R=1

   (That's why this is called the forbidden state.)

B. Q oscillates between 0 and 1 when the inputs transition from 1,1 → 0,0

C. The SR Latch is problematic b/c it has two outputs to store a single bit.

D. There is nothing wrong with the SR Latch!

What's wrong with the SR Latch?

0

Q is undefined when S=1 and R=1 (That's why this is called the forbidden state.)

0%

Q oscillates between 0 and 1 when the inputs transition from 1,1 -> 0,0

0%

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0%

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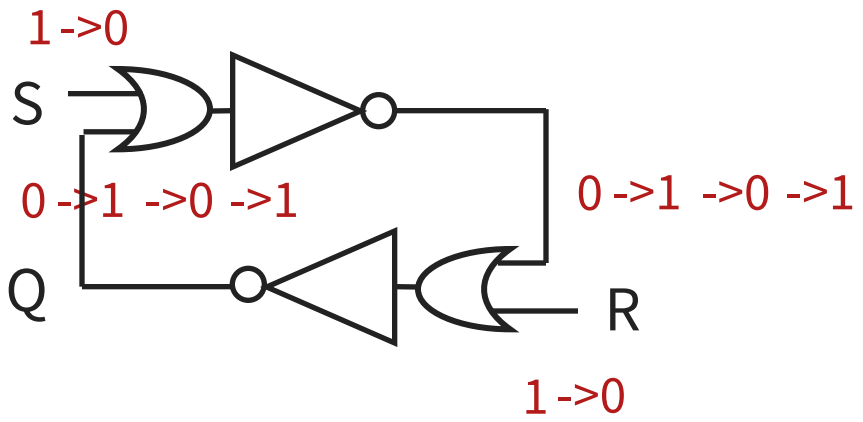
0%

Third Attempt: Set-Reset Latch



A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	forbidden	

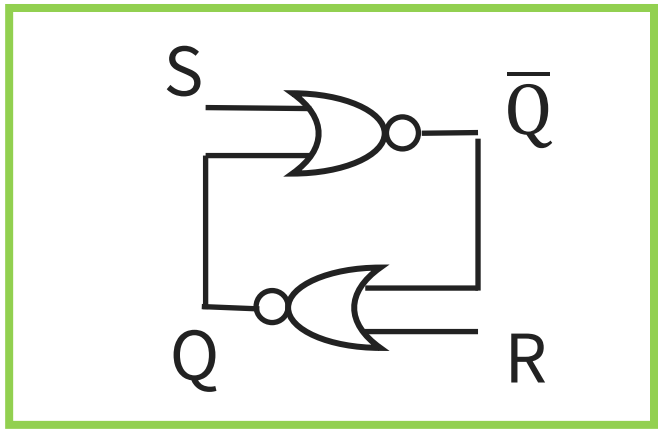
Set-Reset (S-R) Latch

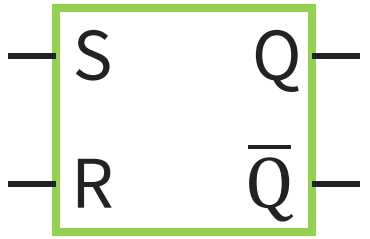
Stores a value Q and its complement

What happens when S,R changes from 1,1 to 0,0?

Q and $\overline{Q}$ become unstable and will oscillate wildly between values 0,0 to 1,1 to 0,0 to 1,1 …

Third Attempt: Set-Reset Latch





S	R	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	hold
0	1	0	1	reset
1	0	1	0	set
1	1	forbidden		

Set-Reset (S-R) Latch
Stores a value Q and its complement

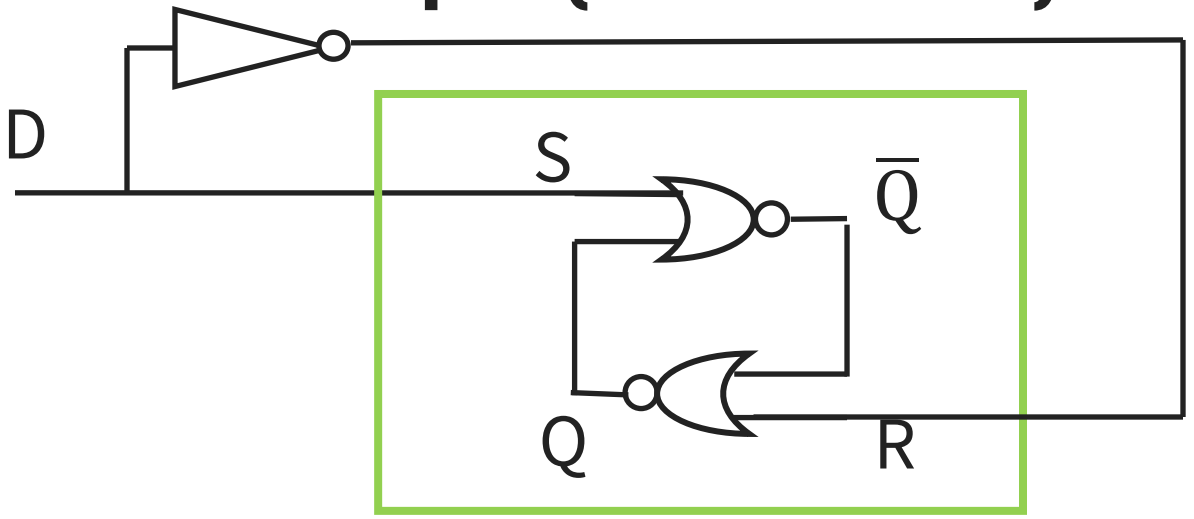
Takeaway

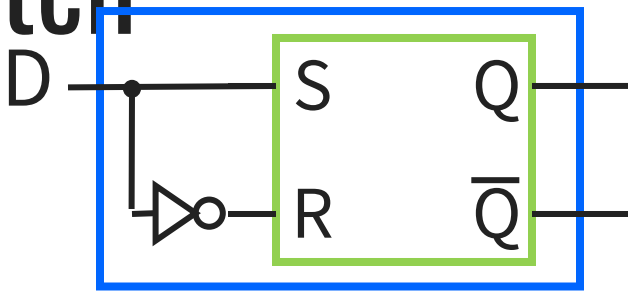
Set-Reset (SR) Latch can store one bit and we can change the value of the stored bit. But, SR Latch has a forbidden state.

Next Goal

How do we avoid the forbidden state of S-R Latch?

Fourth Attempt: (Unclocked) D Latch



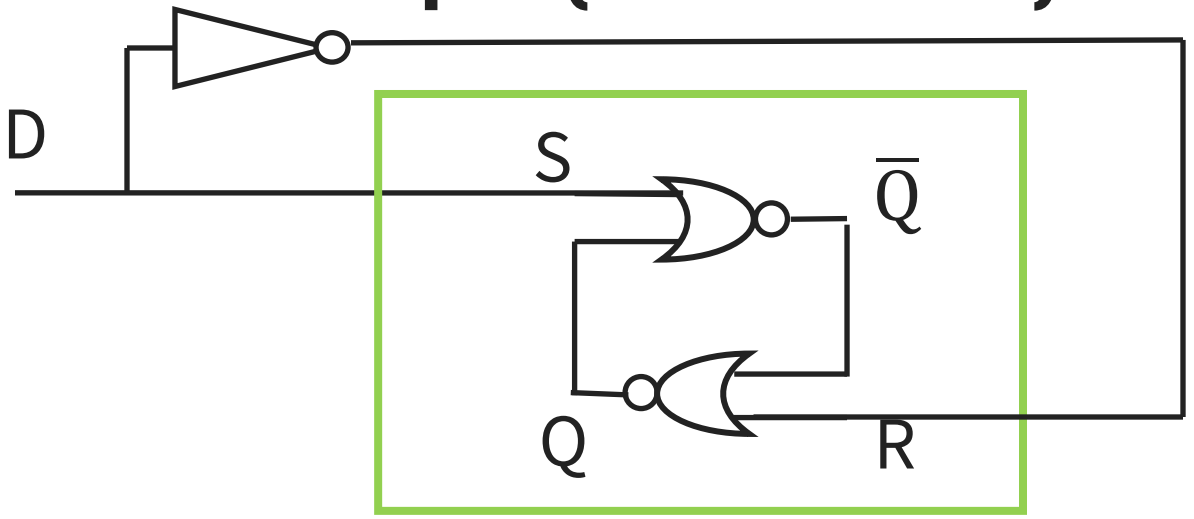


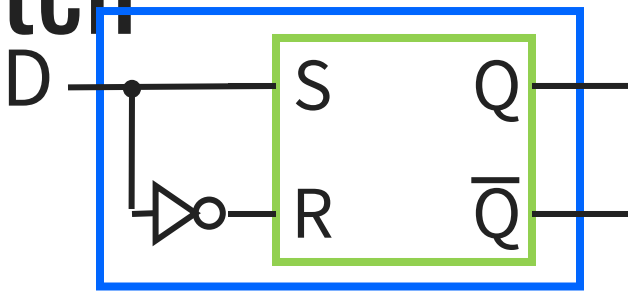
Fill in the truth table?

D	Q	$\overline{Q}$
0		
1		

A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Fourth Attempt: (Unclocked) D Latch





D	Q	$\overline{Q}$
0	0	1
1	1	0

Fill in the truth table?

Data (D) Latch

- Easier to use than an SR latch
- No possibility of entering an undefined state

When D changes, Q changes

- … immediately (…after a delay of 2 Ors and 2 NOTs)

Need to control when the output changes

A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Takeaway

Set-Reset (SR) Latch can store one bit and we can change the value of the stored bit. But, SR Latch has a forbidden state.

(Unclocked) D Latch can store and change a bit like an SR Latch while avoiding the forbidden state.

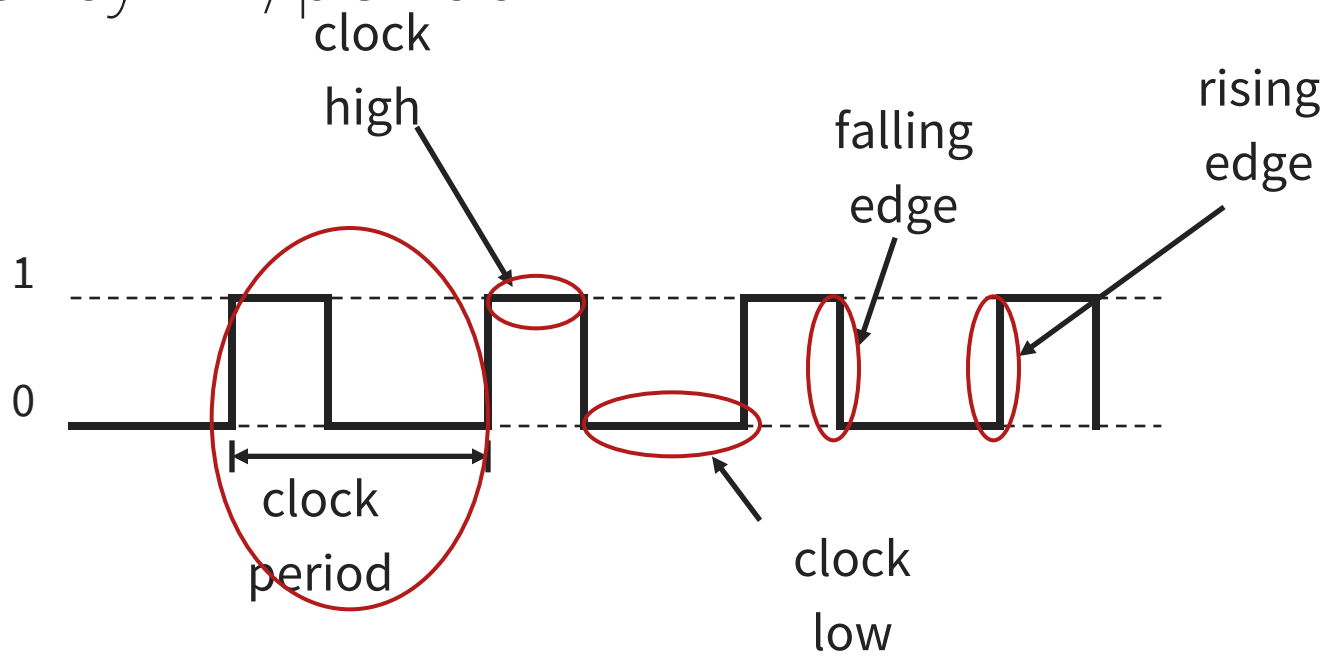
Next Goal

How do we coordinate state changes to a D Latch?

Aside: Clocks

Clock helps coordinate state changes

- Usually generated by an oscillating crystal
- Fixed period
- Frequency = 1/period



Clock Disciplines

Level sensitive

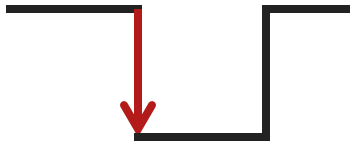
- State changes when clock is high (or low)

Edge triggered

- State changes at clock edge

positive edge-triggered

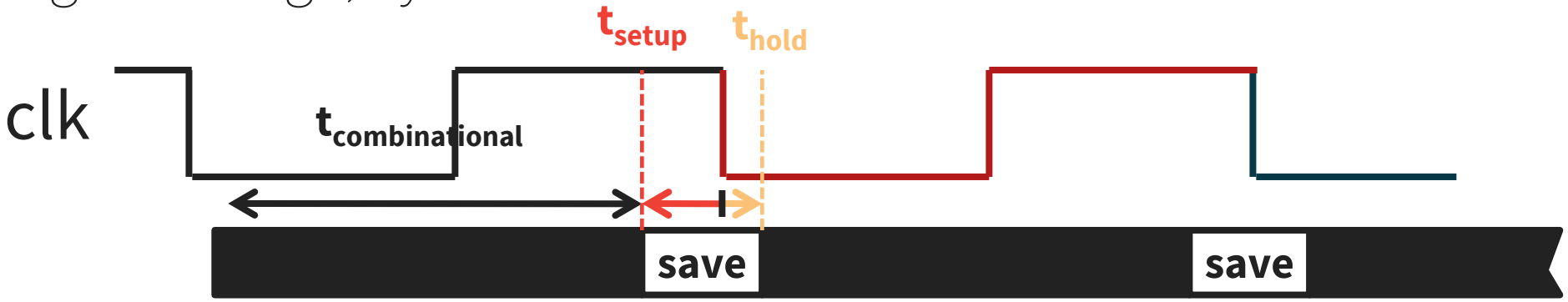
negative edge-triggered



Clock Methodology

Clock Methodology

- Negative edge, synchronous

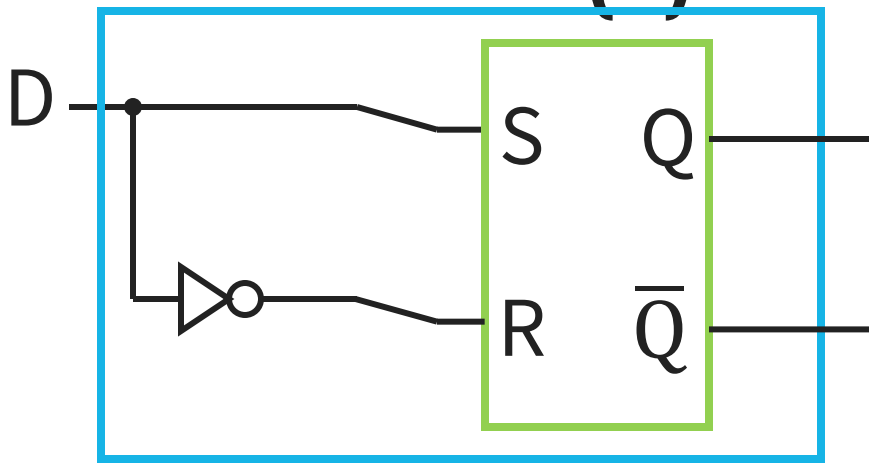


Edge-Triggered → signals must be stable near falling edge

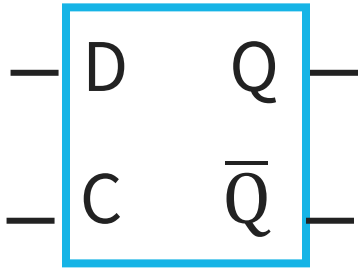
"near" = before and after

t_{setup} t_{hold}

Round 2: D Latch (1)

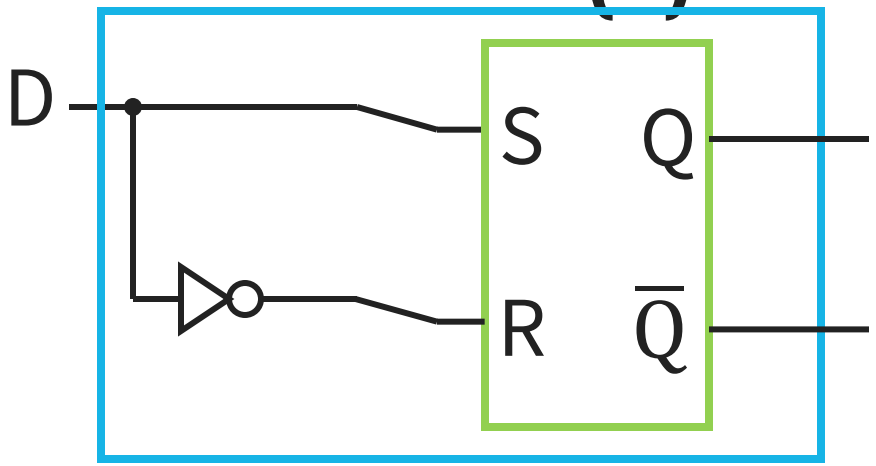


- Inverter prevents SR Latch from entering 1,1 state

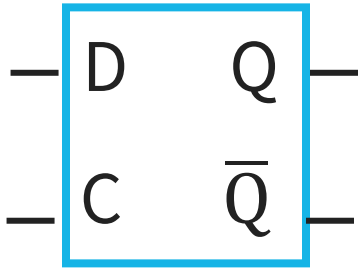


	D	Q	$\overline{Q}$	
	0			*Reset*
	1			*Set*

Round 2: D Latch (1)

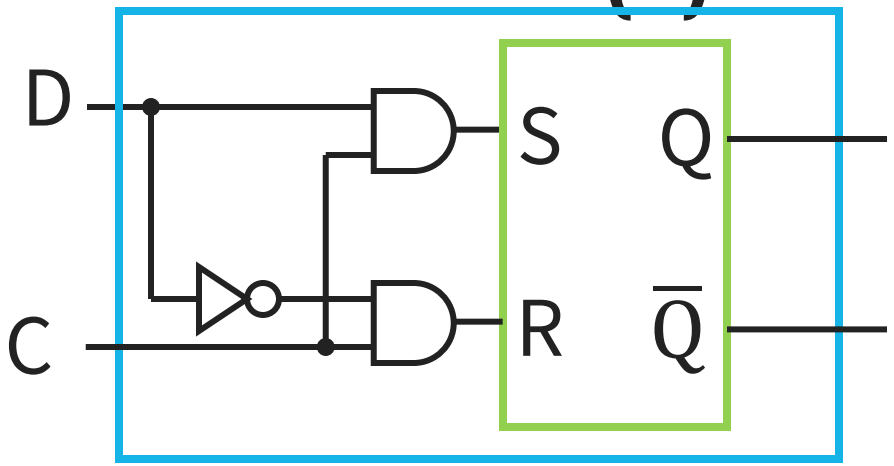


- Inverter prevents SR Latch from entering 1,1 state



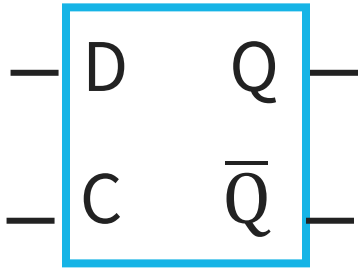
	D	Q	$\overline{Q}$	
	0	0	1	*Reset*
	1	1	0	*Set*

Round 2: D Latch (1)



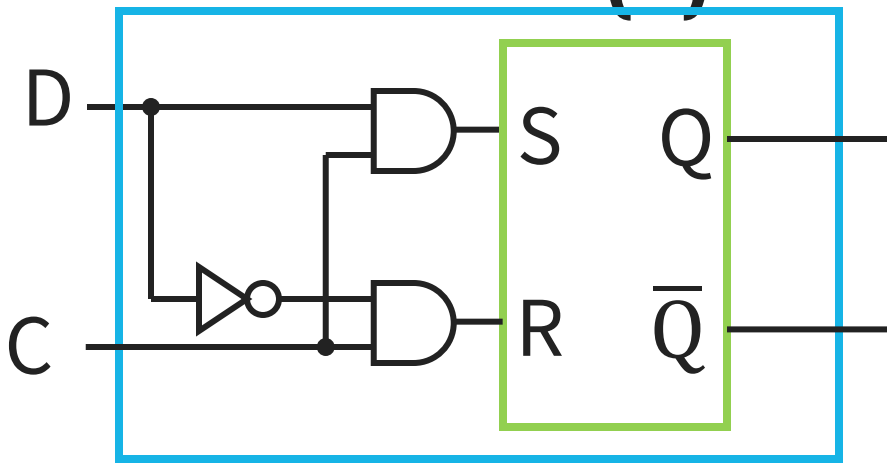
- Level sensitive
- Inverter prevents SR Latch from entering 1,1 state
- C enables changes

C = 1, D Latch *transparent*:
set/reset (according to D)
C = 0, D Latch *opaque*:
keep state (ignore D)



C	D	Q	$\overline{Q}$	
0	0			*No Change*
0	1			
1	0			*Reset*
1	1			*Set*

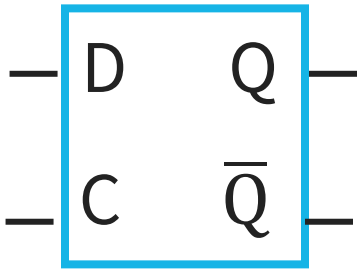
Round 2: D Latch (1)



- Level sensitive
- Inverter prevents SR Latch from entering 1,1 state
- C enables changes

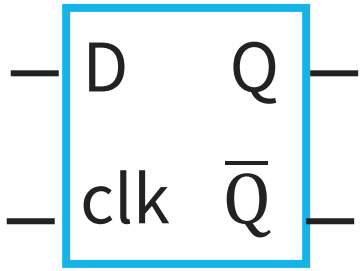
C = 1, D Latch *transparent*:
set/reset (according to D)
C = 0, D Latch *opaque*:
keep state (ignore D)

S	R	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	hold
0	1	0	1	reset
1	0	1	0	set
1	1	forbidden		



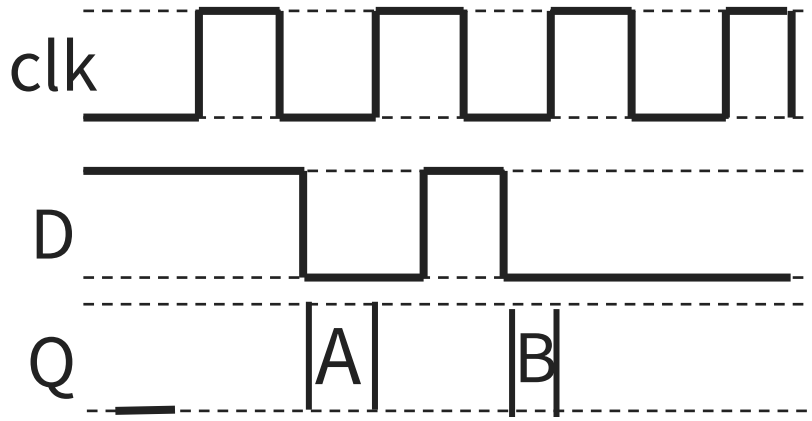
C	D	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	*No Change*
0	1	Q	$\overline{Q}$	
1	0	0	1	*Reset*
1	1	1	0	*Set*

PollEV Question



What is the value of Q at A & B?

a) A = 0, B = 0
b) A = 0, B = 1
c) A = 1, B = 0
d) A = 1, B = 1



clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

What is the value of Q at A & B?

0

A = 0, B = 0

0%

A = 0, B = 1

0%

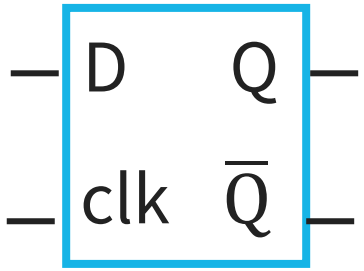
A = 1, B = 0

0%

A = 1, B = 1

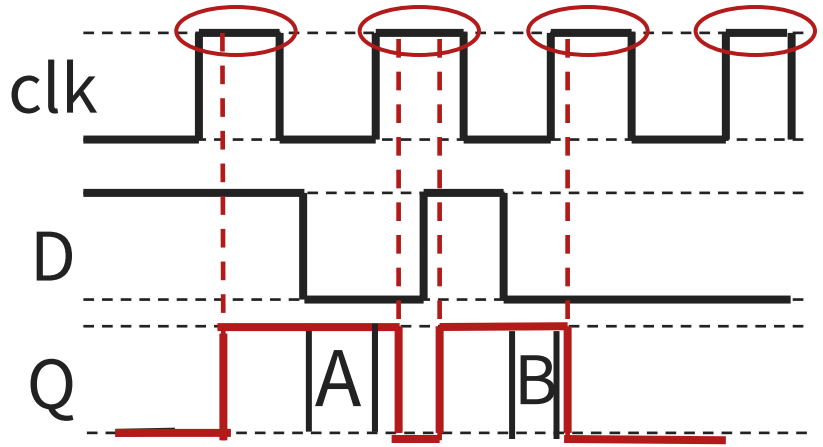
0%

PollEV Question



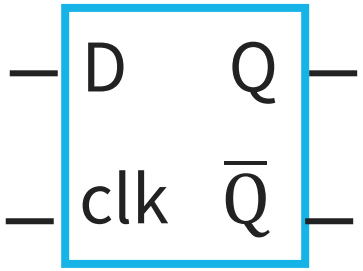
What is the value of Q at A & B?

a) A = 0, B = 0
b) A = 0, B = 1
c) A = 1, B = 0
d) A = 1, B = 1



clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

PollEV Question



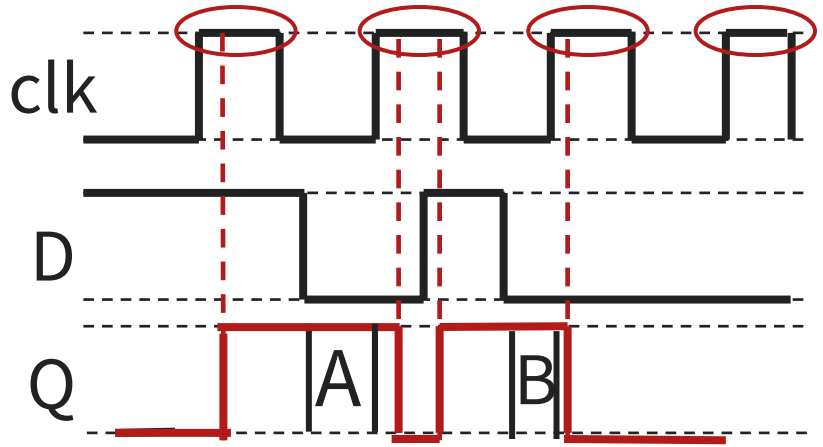
Level Sensitive D Latch

Clock high:

set/reset (according to D)

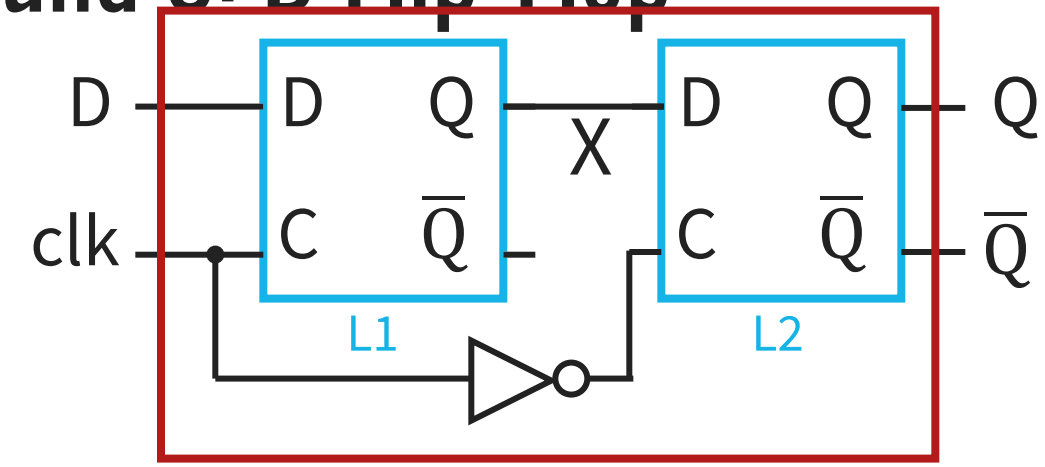
Clock low:

keep state (ignore D)



clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

Round 3: D Flip-Flop



- Edge-Triggered
- Data captured when clock high
- Output changes only on falling edges

Round 3: D Flip-Flop

Clock = 1: L1 *transparent*

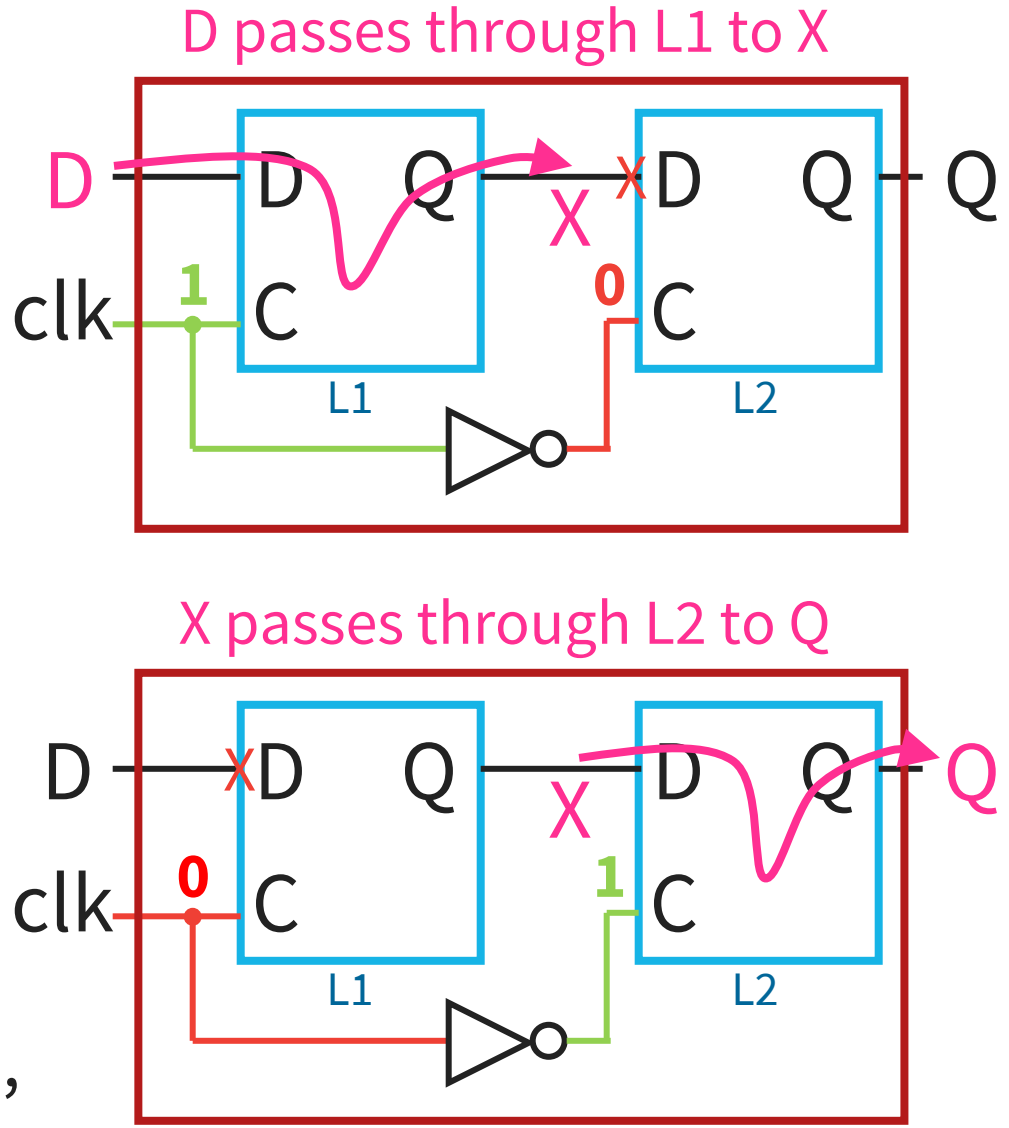
L2 *opaque*

When CLK rises (0→1), now X can change, Q does not change

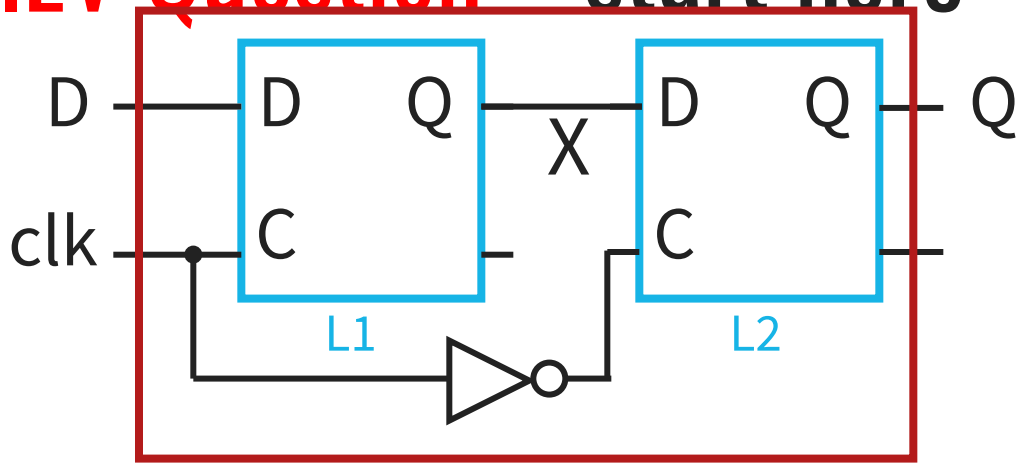
Clock = 0: L1 *opaque*

L2 *transparent*

When ***CLK* falls** (1→0), *Q gets X, X cannot change*

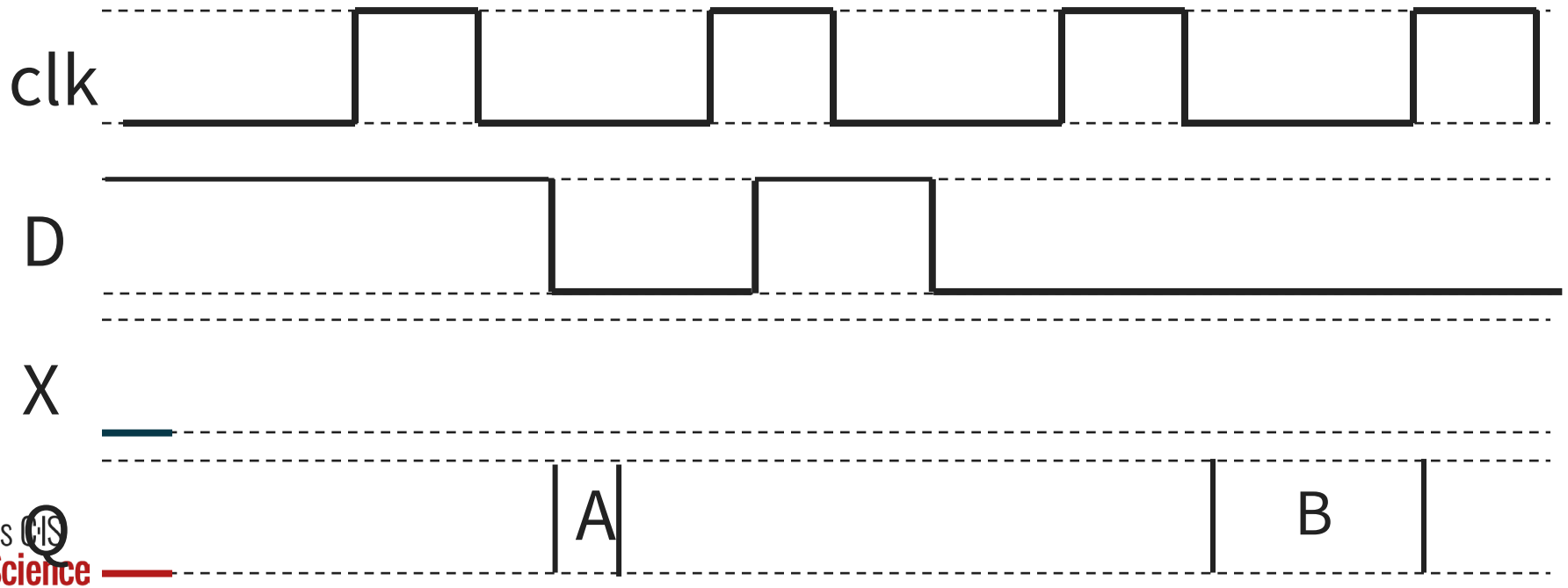


PollEV Question – start here



What is the value of Q at A & B?

a) A = 0, B = 0
b) A = 0, B = 1
c) A = 1, B = 0
d) A = 1, B = 1



What is the value of Q at A & B? (take two)

0

A = 0, B = 0

0%

A = 0, B = 1

0%

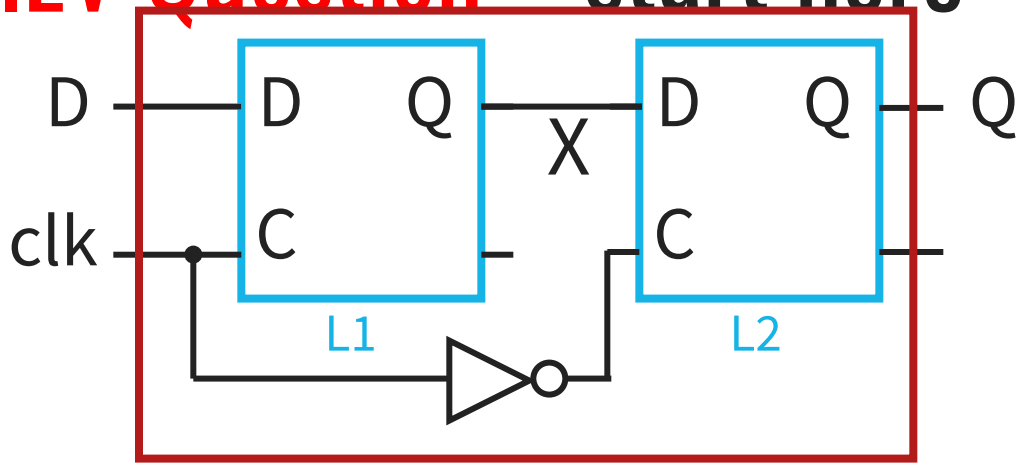
A = 1, B = 0

0%

A = 1, B = 1

0%

PollEV Question – start here



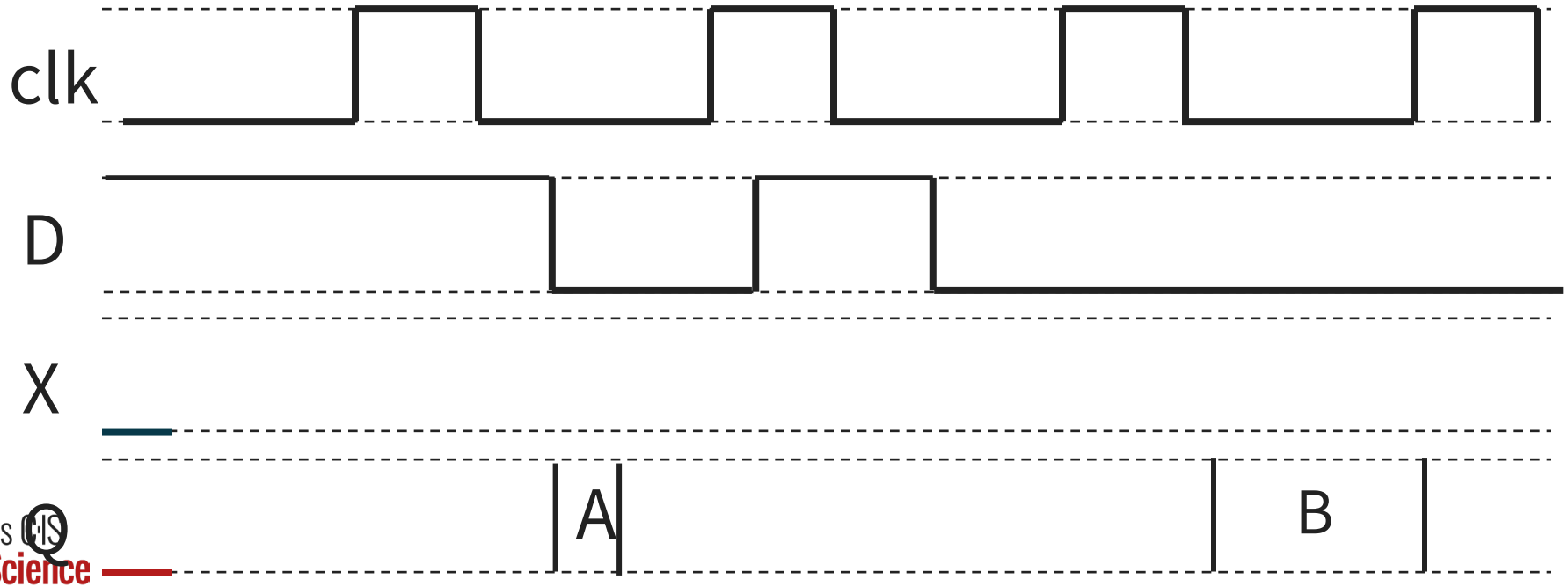
What is the value of Q at A & B?

a) A = 0, B = 0

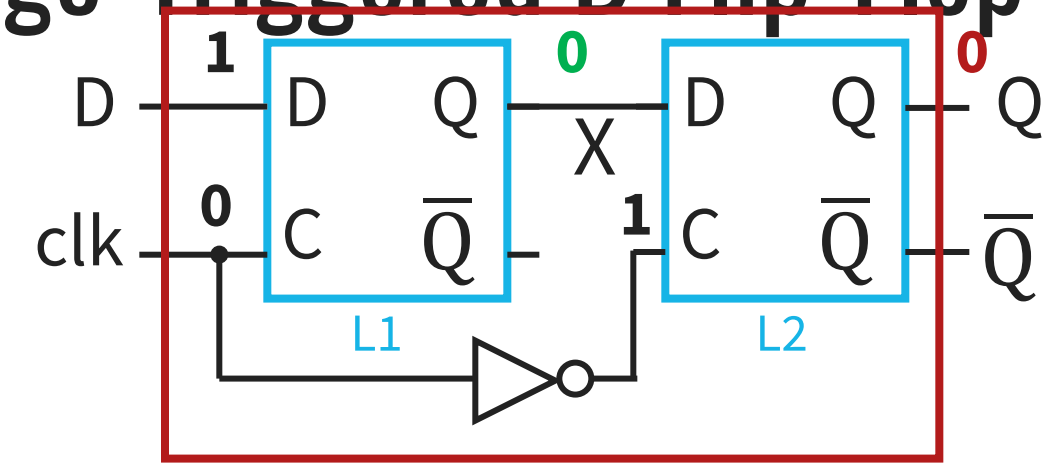
b) A = 0, B = 1

c) A = 1, B = 0

d) A = 1, B = 1

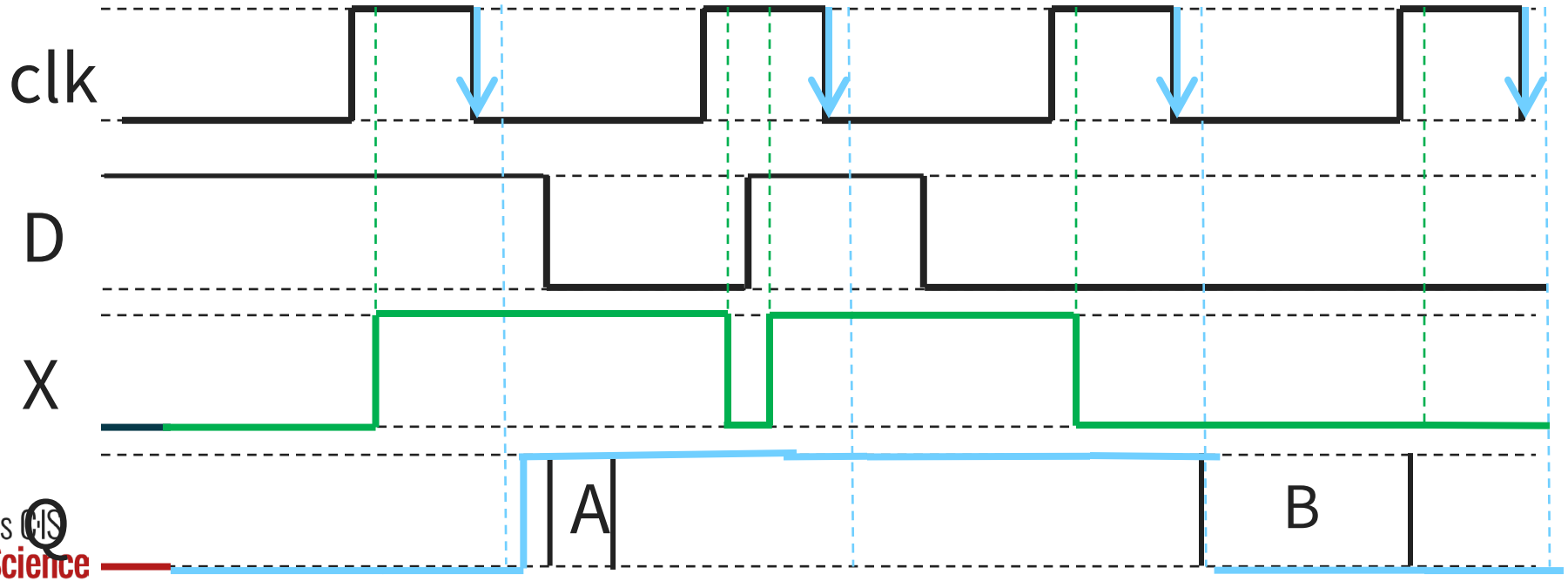


Edge-Triggered D Flip-Flop

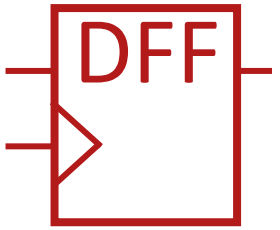


D Flip-Flop

- Edge-Triggered
- Data captured when clock is high
- Output changes only on falling edges

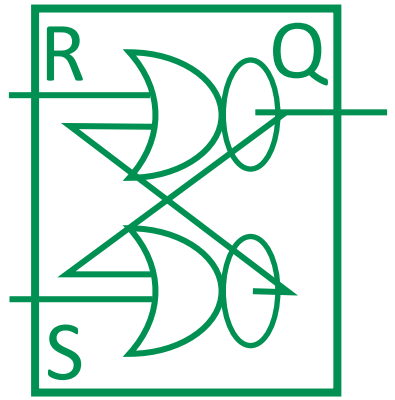


Building a D Flip Flop (DFF)

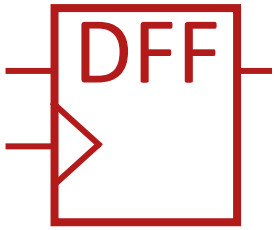


Step 1: Create an SR Latch

Set	Reset	Q
0	0	Q
0	1	0
1	0	1
1	1	?



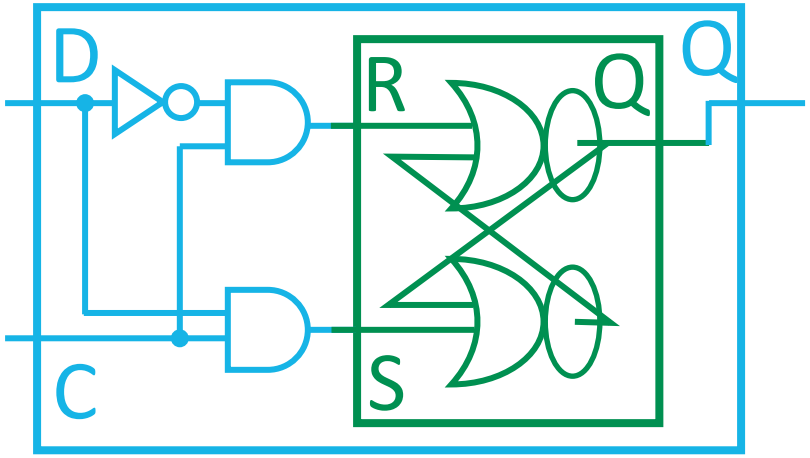
Building a D Flip Flop (DFF)



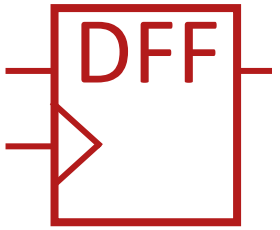
Step 1: Create an SR Latch

Step 2: Create a D Latch

Clk	Data	Q
0	0	Q
0	1	Q
1	0	0
1	1	1



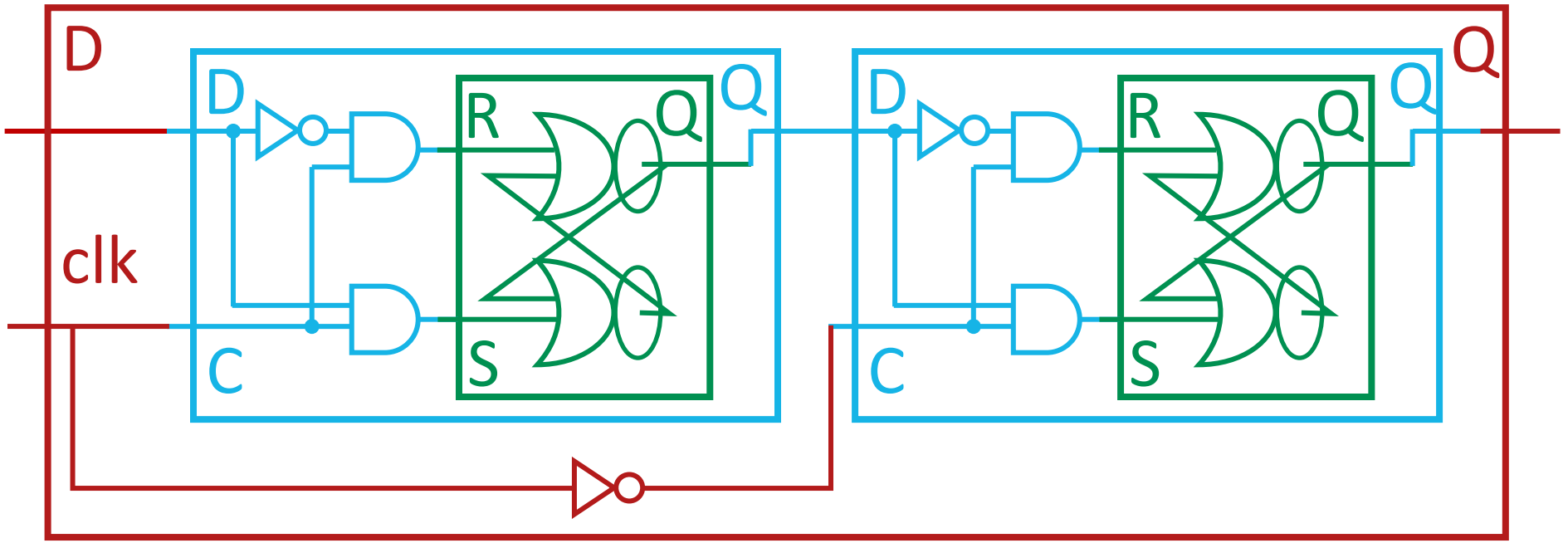
Building a D Flip Flop (DFF)



Step 1: Create an SR Latch

Step 2: Create a D Latch

Step 3: Duplicate the D Latch, chain together



Takeaway

Set-Reset (SR) Latch can store one bit and we can change the value of the stored bit. But, SR Latch has a forbidden state.

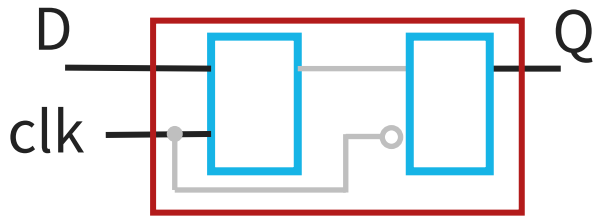
(Unclocked) D Latch can store and change a bit like an SR Latch while avoiding a forbidden state.

An Edge-Triggered D Flip-Flip (aka Master-Slave D Flip-Flip) stores one bit. The bit can be changed in a synchronized fashion on the edge of a clock signal.

Next Goal

How do we store more than one bit, N bits?

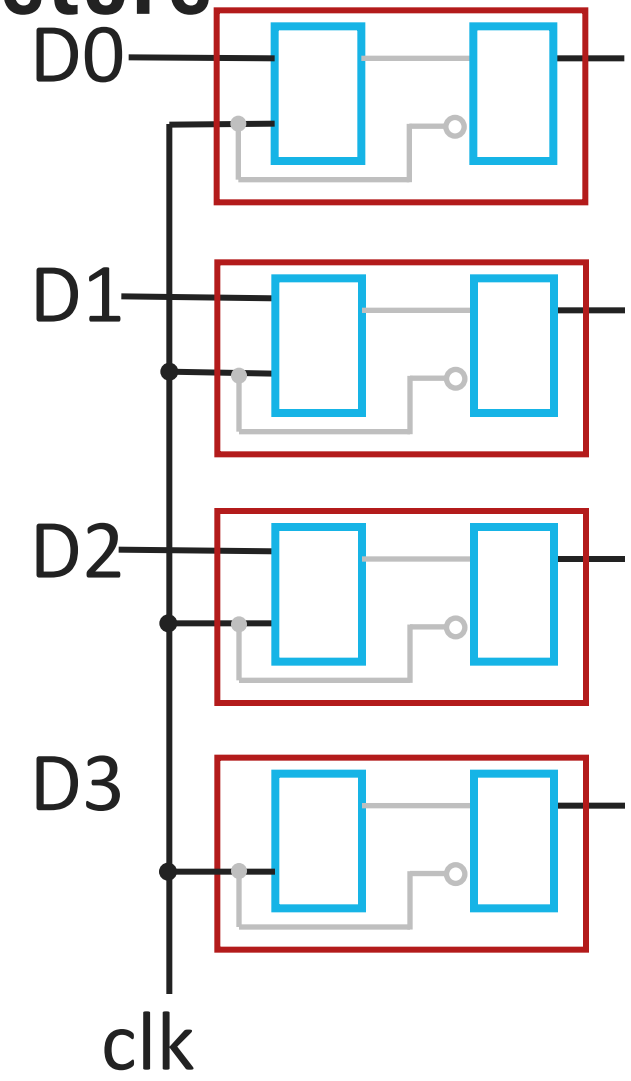
Registers



Register

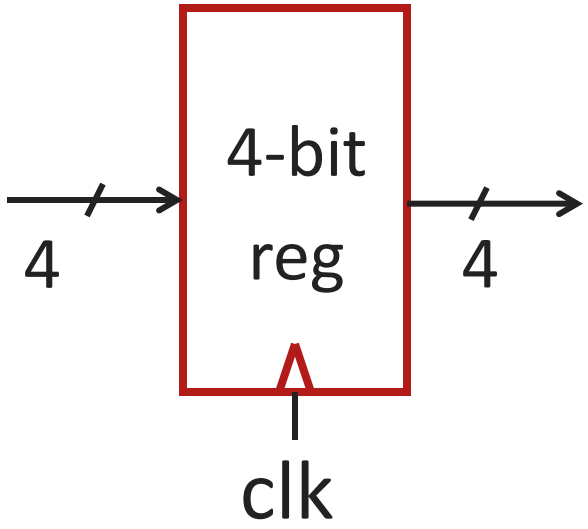
- D flip-flops in parallel

Registers

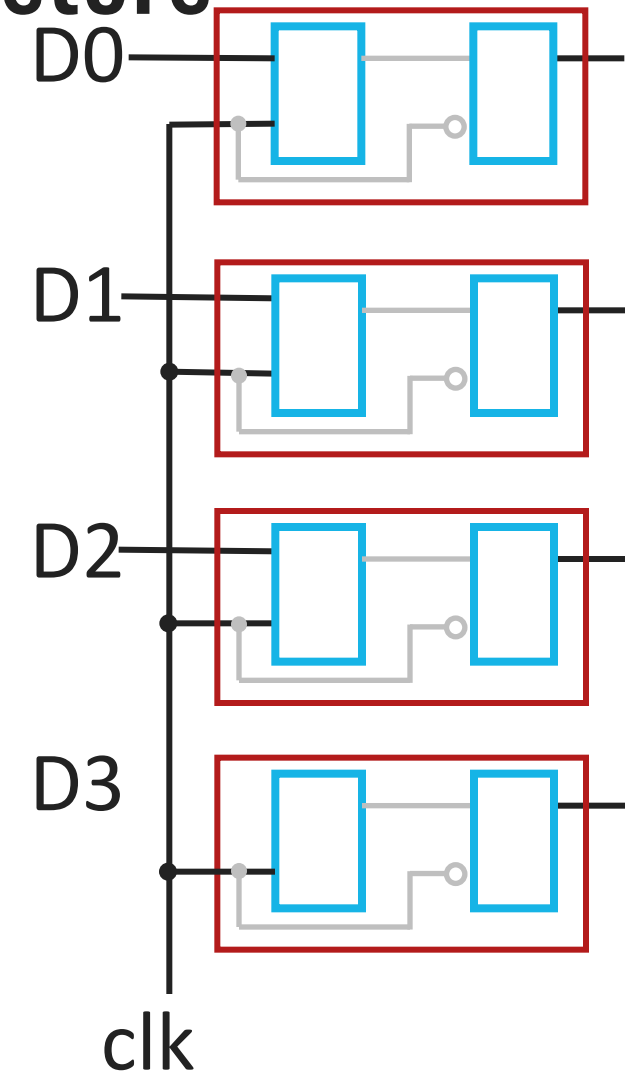


Register

- D flip-flops in parallel
- shared clock
- extra clocked inputs: write_enable, reset, …



Registers



Register

- D flip-flops in parallel
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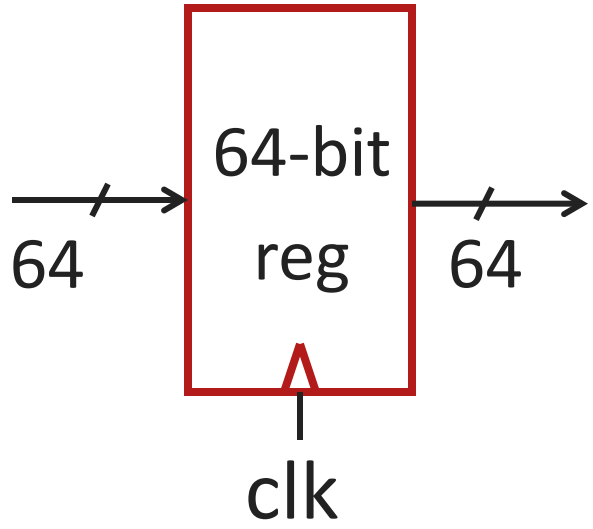

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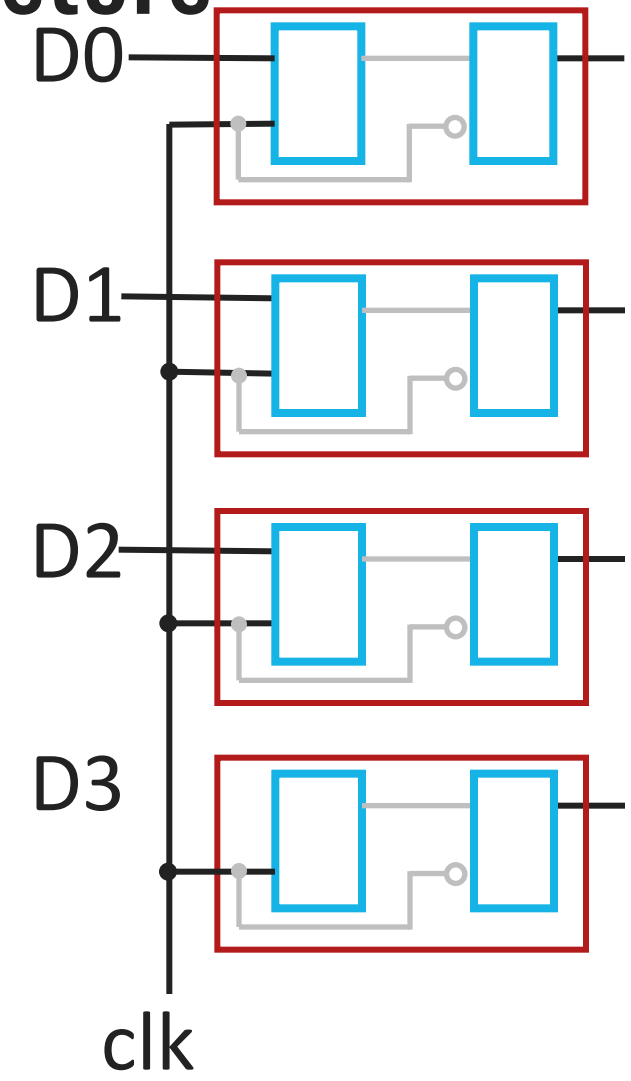
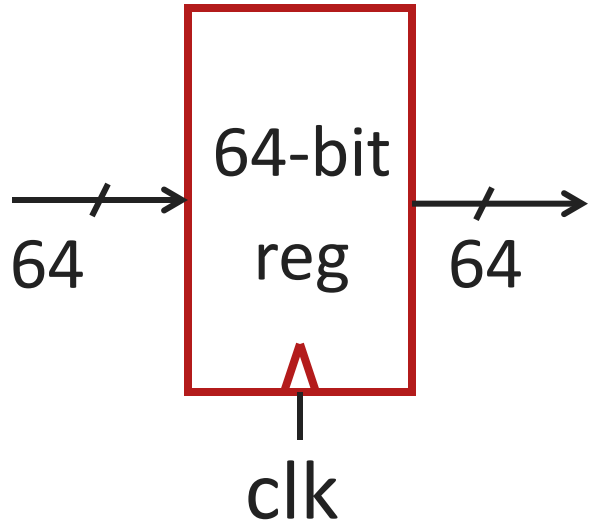
An *N*-bit register stores *N*-bits. It is created with *N* D-Flip-Flops in parallel along with a shared clock.

Registers

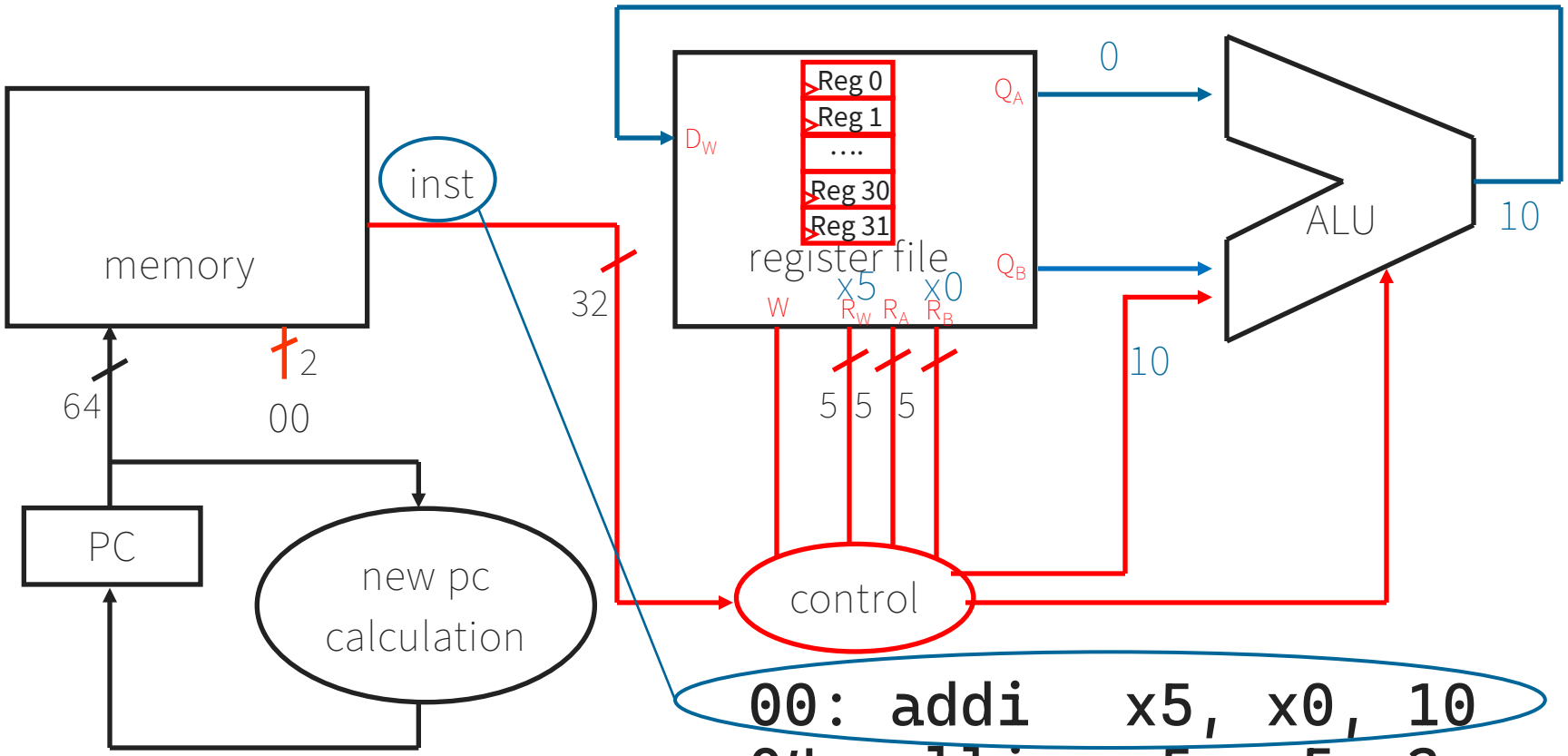


Register

- D flip-flops in parallel
- shared clock
- extra clocked inputs: write_enable, reset, …



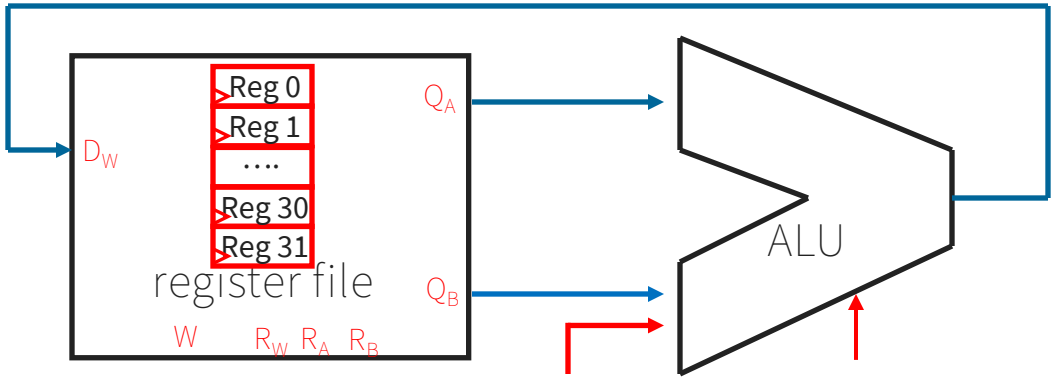
Big Picture: How to Design a Processor



Big Picture: How to Design a Processor

Register File

- N read/write registers
- Indexed by register number

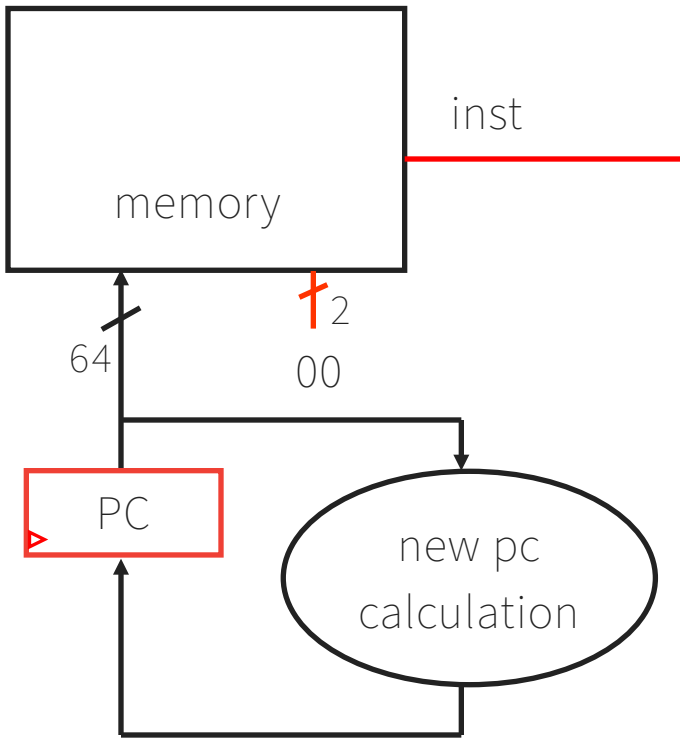


Registers

- Numbered from 0 to 31
- Can be referred by number: x0, x1, x2, … x31
  - May also see $0, $1, $2 or r0, r1, r2
- Convention, each register also has a name:
  - x16 - x23 → s0-s7 ("s registers")
  - x8 - x15 → t0 - t7 ("t registers")

```
00: addi   x5, x0, 10
04: slli   x5, x5, 2
08: addi   x5, x5, 15
```

Big Picture: How to Design a Processor

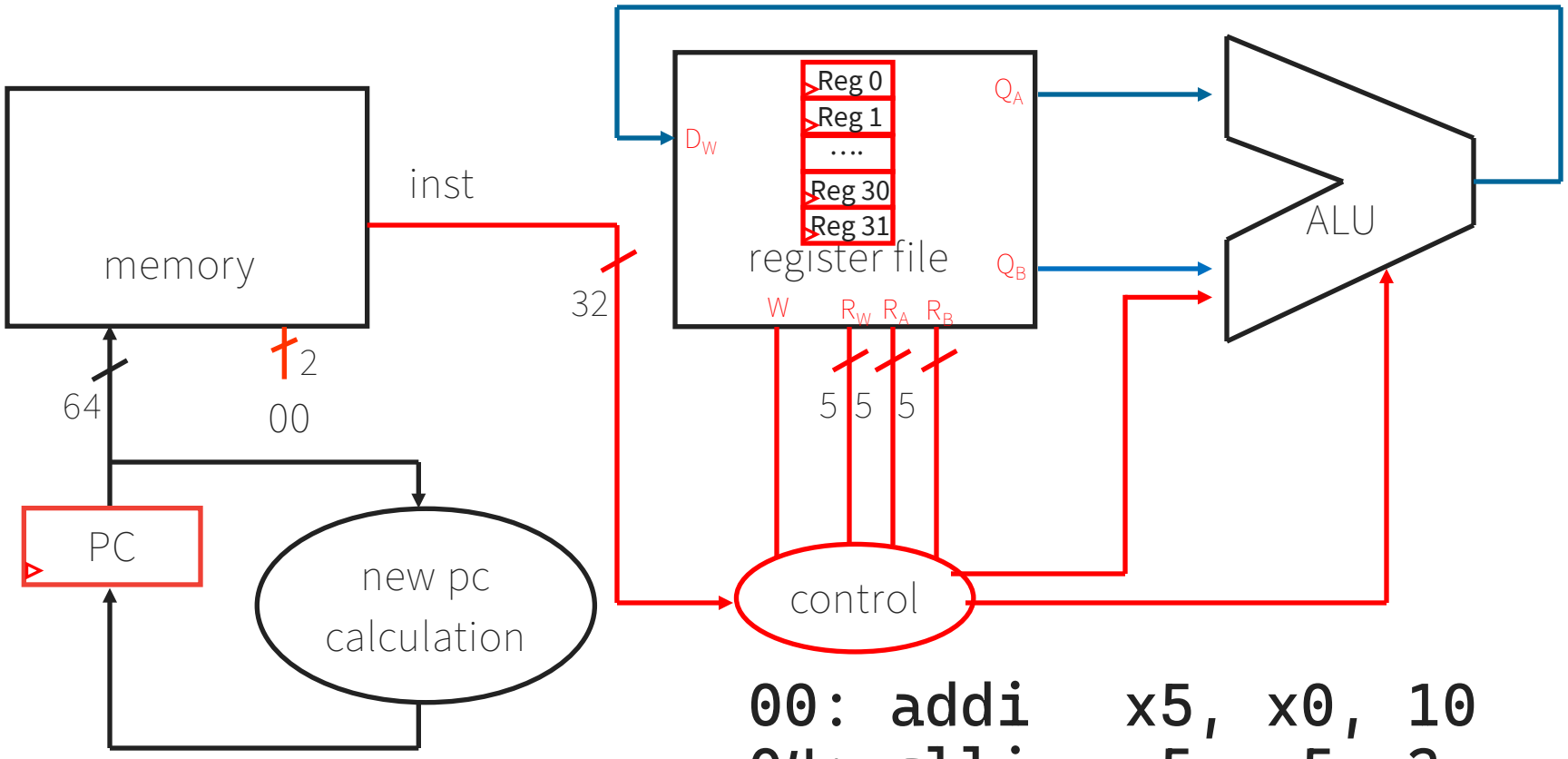


PC is register!

- PC is the Program Counter
- Stores the memory address of the next instruction

```
00: addi   x5, x0, 10
04: slli   x5, x5, 2
08: addi   x5, x5, 15
```

Big Picture: How to Design a Processor

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An *N*-bit register stores *N*-bits. It is created with *N* D-Flip-Flops in parallel along with a shared clock.

Summary

We store data values

- Stateful circuit elements (D Flip Flops, Registers, …)
- Clock to synchronize state changes